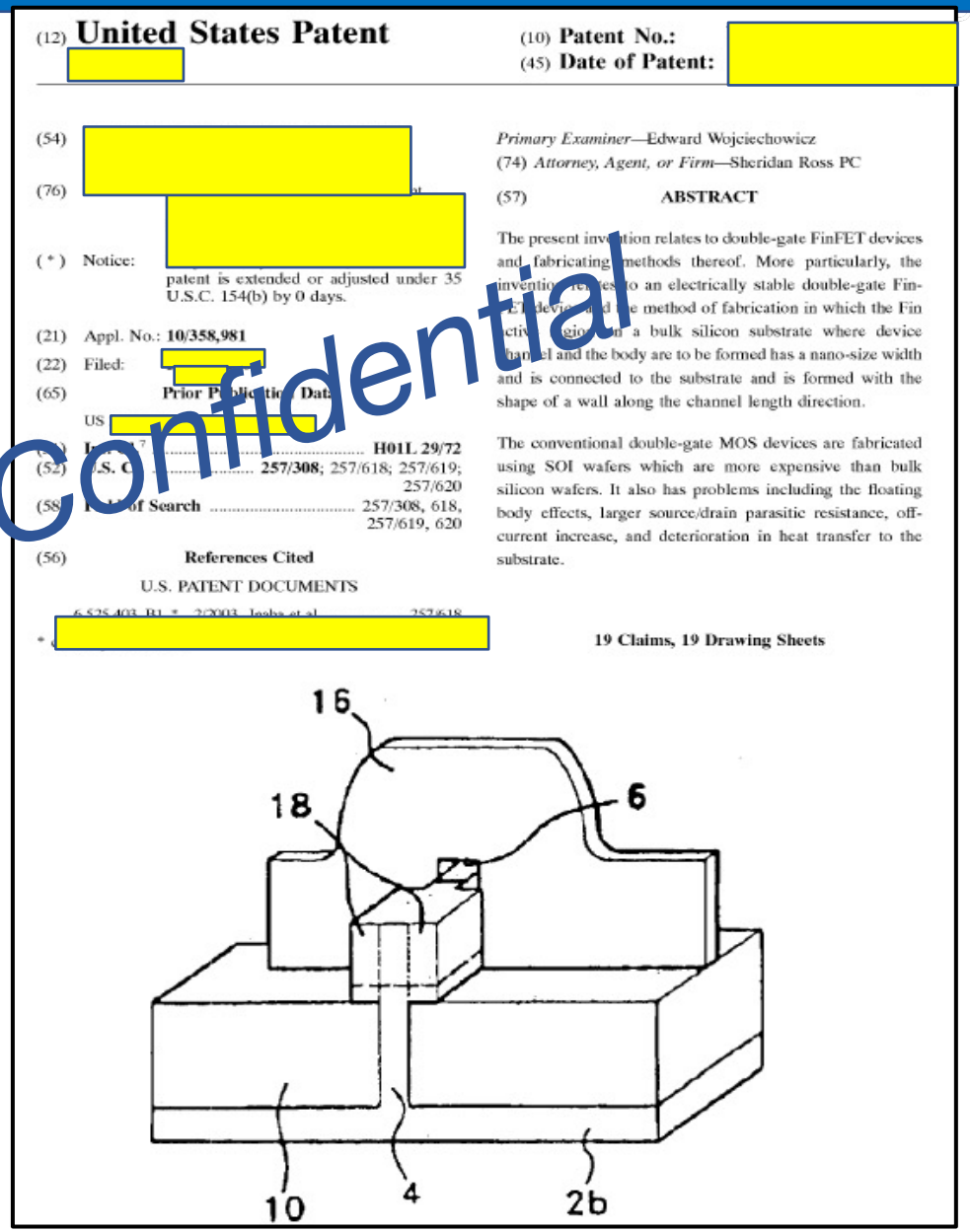
US Patent X,XXX,XXX

Outermost Technology

- Title:
- Inventor:
- Priority Dates
  - Priority Date & Filing Date: 2003
  -
- Exemplary Claim: claim 1 ~ 4
- Illustrative Products:
  - Mini Applications Processor products with the part ID
  - Other chips made using 14nm finFET process



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(45) **Date of Patent:**

(54)
(76)
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US
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(52) U.S. C. **257/308**; 257/618; 257/619; 257/620
(58) Field of Search 257/308, 618, 257/619, 620

(56) **References Cited**
U.S. PATENT DOCUMENTS

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(57) **ABSTRACT**

The present invention relates to double-gate FinFET devices and fabricating methods thereof. More particularly, the invention relates to an electrically stable double-gate FinFET device and the method of fabrication in which the Fin active region on a bulk silicon substrate where device channel and the body are to be formed has a nano-size width and is connected to the substrate and is formed with the shape of a wall along the channel length direction.

The conventional double-gate MOS devices are fabricated using SOI wafers which are more expensive than bulk silicon wafers. It also has problems including the floating body effects, larger source/drain parasitic resistance, off-current increase, and deterioration in heat transfer to the substrate.

19 Claims, 19 Drawing Sheets