Innovation Together

Outermost Technology

SoC Process Sample Report

14 nm FinFET SoC XXX

March 2022

Report ID: 2008-13263

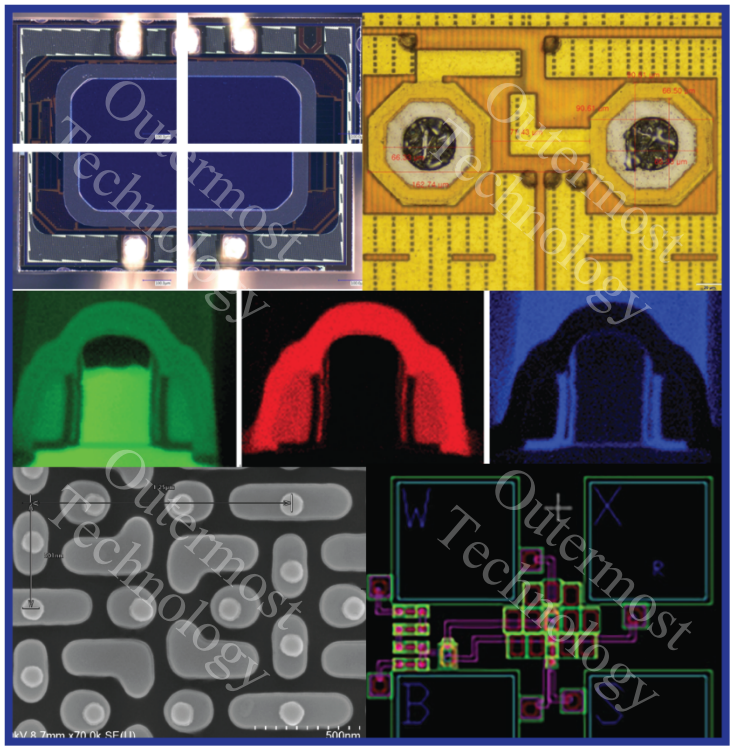

Table of Contents

Device Summary Table

Manufacturer	XXX
Part Number	XXXXXXXXXXXXX
Part Description	Mini application processor
Package Size	14 mm x 14 mm = 196 mm²
Package Type	485 ball FBGA (fine pitch Ball Grid Array)
Package Markings (top)	XXXXXXXXX
Die Markings	XXXXXXX
Die Size	4.75 mm x 3.83 mm = 18.19 mm²
Die Thickness	140 µm
Number of Metal Levels	12
Number of Metal Gate Levels	1
Foundry	Samsung
Foundry Process Node	14LPC
Process Generation	14 nm
Process Type	CMOS (Copper)
Feature Measured to Determine Process Generation	Fin pitch, contacted gate pitch, metal 2 pitch, SRAM cell size
Transistor Gate Length	30 nm & 33 nm (PMOS & NMOS Logic)
SRAM Cell Size	0.0797 µm²
Transistor FinFET Pitch	49 nm
Transistor Gate Pitch	78 nm
BEOL Process	12 metals (11 Cu + 1 Al) process
Minimum Metal Pitch	67 nm

Process Summary Table

Level	Materials	Process
Substrate	Silicon	Lightly doped bulk P-type silicon (Si) substrate.
Wells	Silicon (*)	Assumed twin-well process with likely multiple implants followed by annealing (not analyzed).
Fin and Isolation	Silicon, SiO2	1st shallow trench isolation (STI) used to define fin and additional etch to remove non-active fins and to create deep STI. An SiOx is filled in defined STI and polished. Thermal oxidation to repair etch-induced damage and define silicon fin profile.
Sacrificial Gate	Polysilicon (*)	A typical gate last process is assumed. Grow thin oxide layer on Si fins, and deposit sacrificial polysilicon gate layer. then pattern and etch sacrificial polysilicon. A double patterning with 193 nm litho, assumed LELE (Litho Etch Litho etch) option is likely used to define minimum 30 nm PMOS & 33 nm NMOS poly gate length and 78 nm contacted gate pitch.
NMOS Source/Drain (S/D)	e-Si epi	Pattern and expose NMOS S/D; etch to form silicon cavity; Si selective epitaxial growth.
PMOS Source/Drain (S/D)	e-SiGe epi	Pattern and expose PMOS S/D; etch to form silicon cavity; SiGe selective epitaxial growth, graded Ge concentration from top to bottom.
Contact Etch Stop Layer S (CESL)	SiON	Deposition of a conformal nitride layer as a contact etch stop layer and the metal gate capping on top of the polished metal gates.
PMD	SiOx/SiCxNy/ SiOx/SiCxNy	Conformal SiN CESL + SiOx 1st PMD + SiCN etch stop layer for the local interconnect(2nd PMD) + SiOx 3rd PMD + SiCN 4th PMD layers.
Interfacial Gate Dielectric	SiOx	After removal of sacrificial poly gates, form SiO_2 prior to deposition of high-k gate dielectric HfOx.
High-k Gate Dielectric	HfOx	Atom layer deposition (ALD) HfOx on thin SiOx interface oxide layer followed by likely post-deposition annealing.
PMOS Metal Gate	TiN/TiAlC/TiN/W; (W not visible)	PMOS work function(WF) layer TiN which is likely removed during NMOS formation; TiN capping layer & gate fill by W. However W fill in the middle of the gates is not visible due to the gap enclosure.

Level	Materials	Process
NMOS Metal Gate	AlTiC/TiN/W; (W not visible)	After PMOS gates are formed and likely removed from NMOS area, and then TiAlC NMOS WF layer is deposited and followed by TiN capping layer & W gate fill even though W fill is not visible in the gates.
Contact	W	SiOx to cover the metal gates and then planarized before the formation of the contact; CVD W plug with Ti/TiN liner.
Metal 1 to Metal 11, Via 0 to Via 10	Cu with Ta/TaN Barrier	Dual damascene copper process, Ta deposited for the barrier layer and a sligth trace of TaN is also foind. It is not clear TaN is deposited separately or formed by reaction with SiCN.
Metal 12 & Via 11	Al with TaN Barrier and ARC	PVD sputter Al deposition; Al dry etch
ILD 0 to ILD 8	SiCxNy/SiOx/SiOxCy	CVD SiCN capping layer; silicon oxide adhesion layer; high-k SiOC between metal lines.
ILD 9	SiCN/SiO2/SiN/SiO2	CVD deposit four layers
ILD 10	SiN/SiO2/SiN/SiO2	CVD deposit four layers
Passivation	SiO2/SiN	CVD

1.0 Package and Die Overview

1.1 Package Overview

Feature	Dimension	Unit
Package Marking	XXXXXXXXX ON14Y SBAG1948A	-
Package Size	14 x 14	mm
Ball Count	486	EA
Ball Size	307	um
Ball Pitch	506	um

Figure 1.1.1: Package summary

Figure 1.1.2: Package (top) image

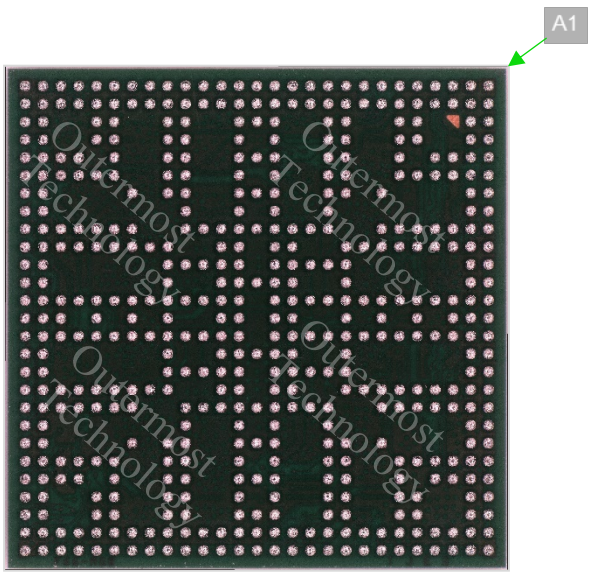

Figure 1.1.3: Package (bottom) image

Figure 1.1.4: Package (Measurement)

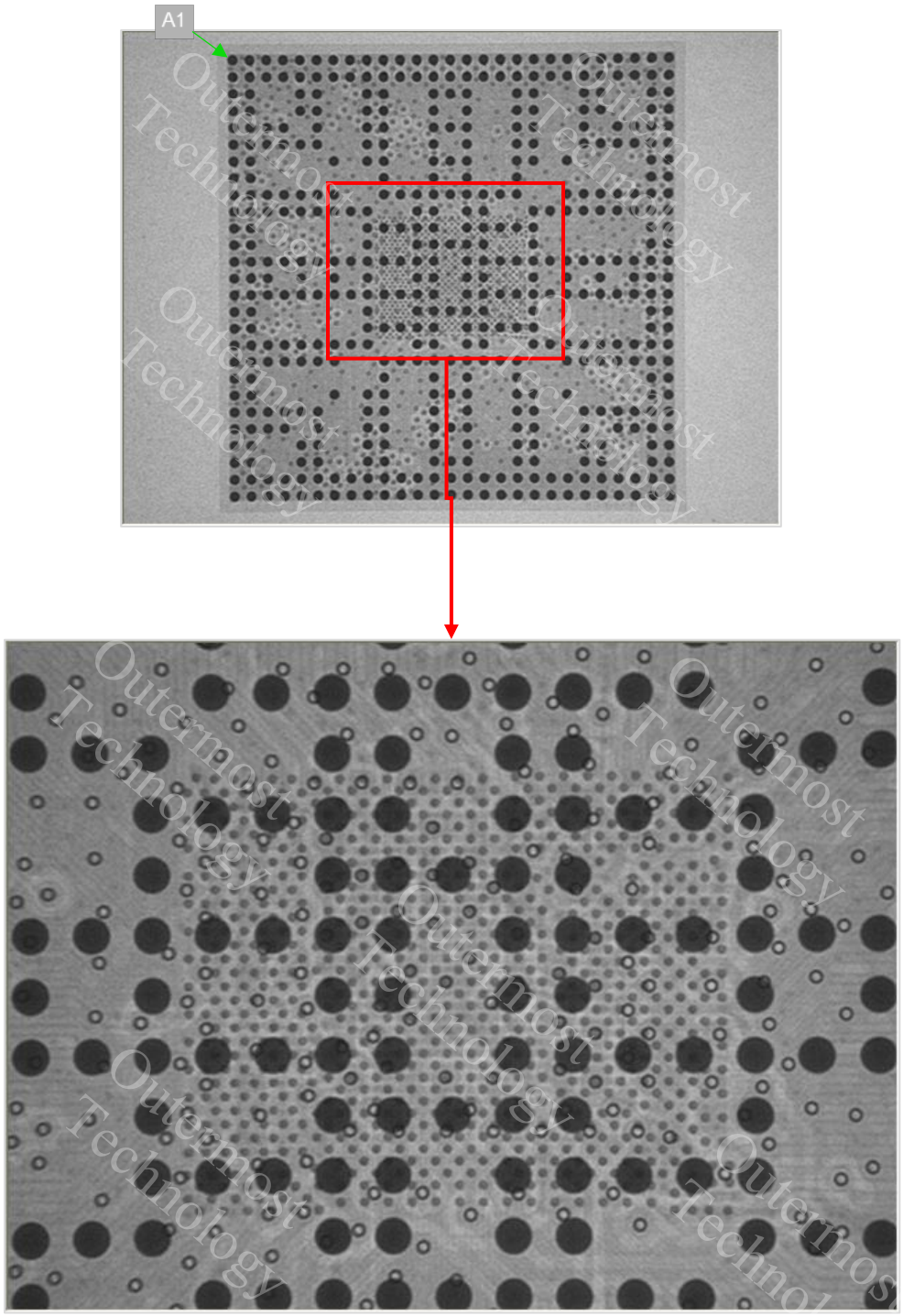

Figure 1.1.5: Package X-ray image

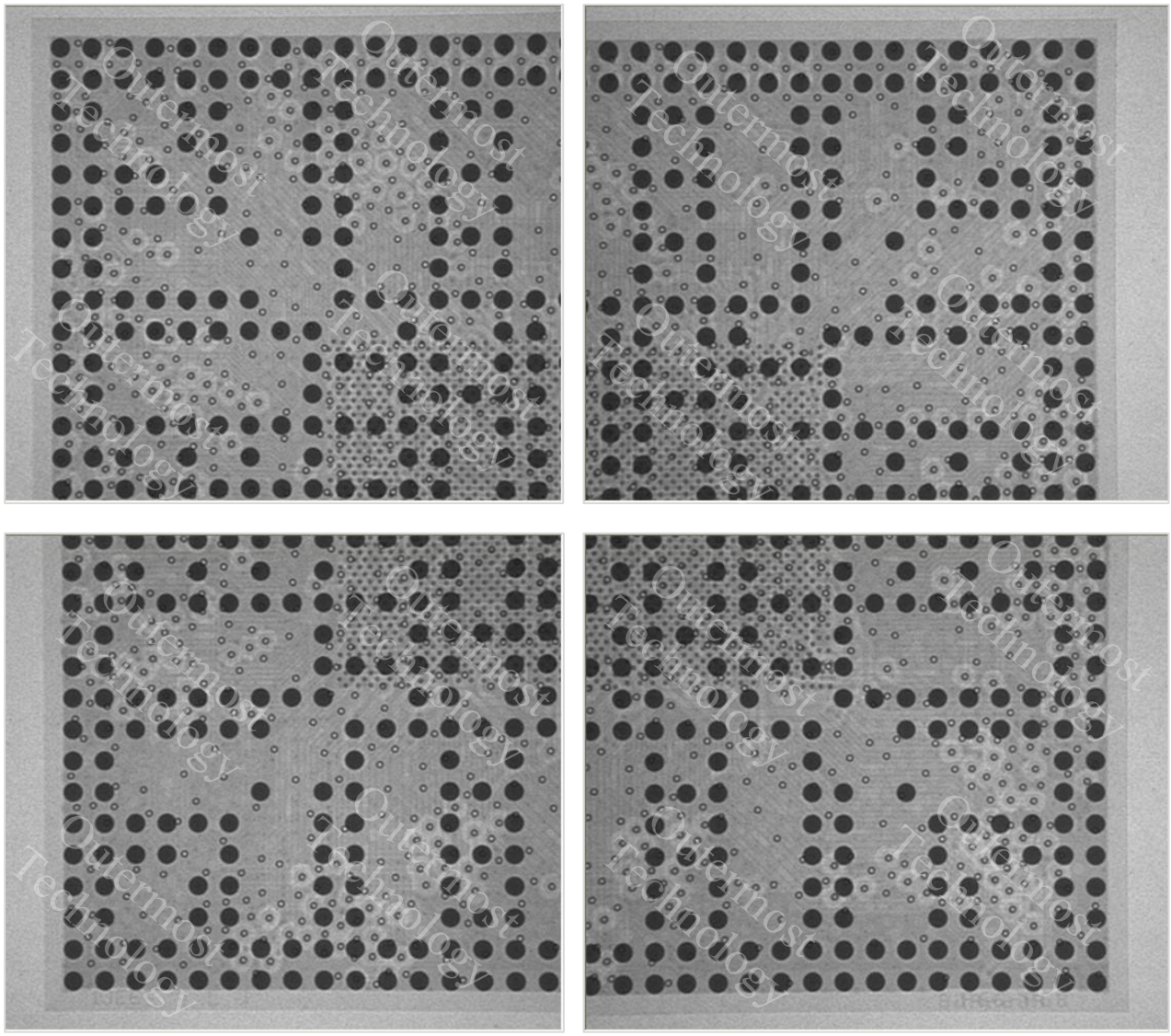

Figure 1.1.6: Package X-ray image

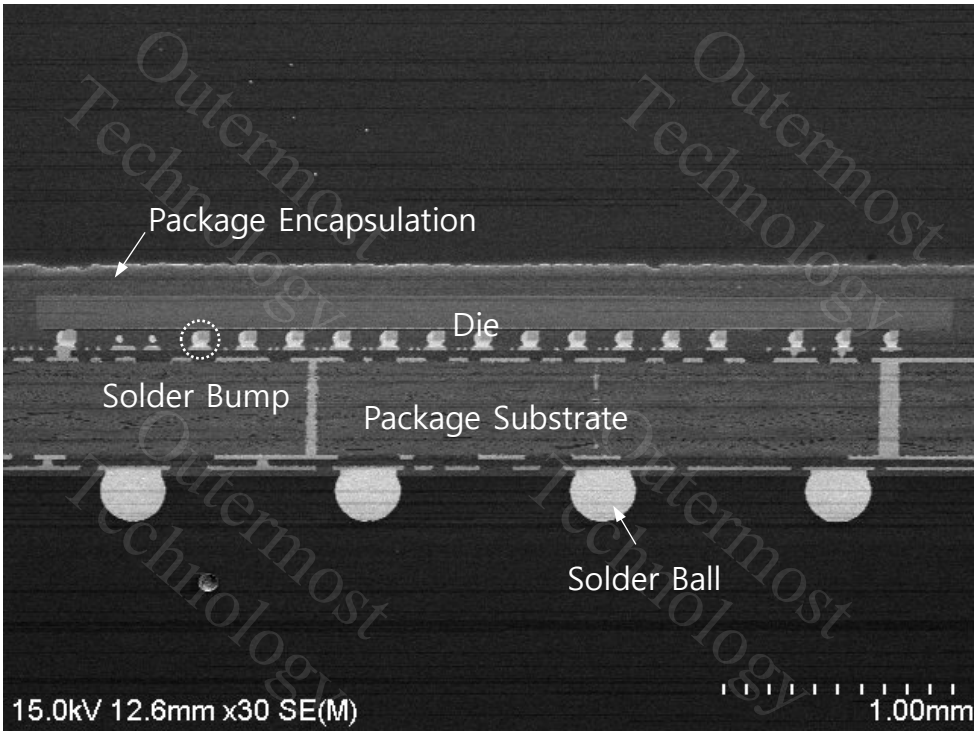

Figure 1.1.7: package cross sectional image

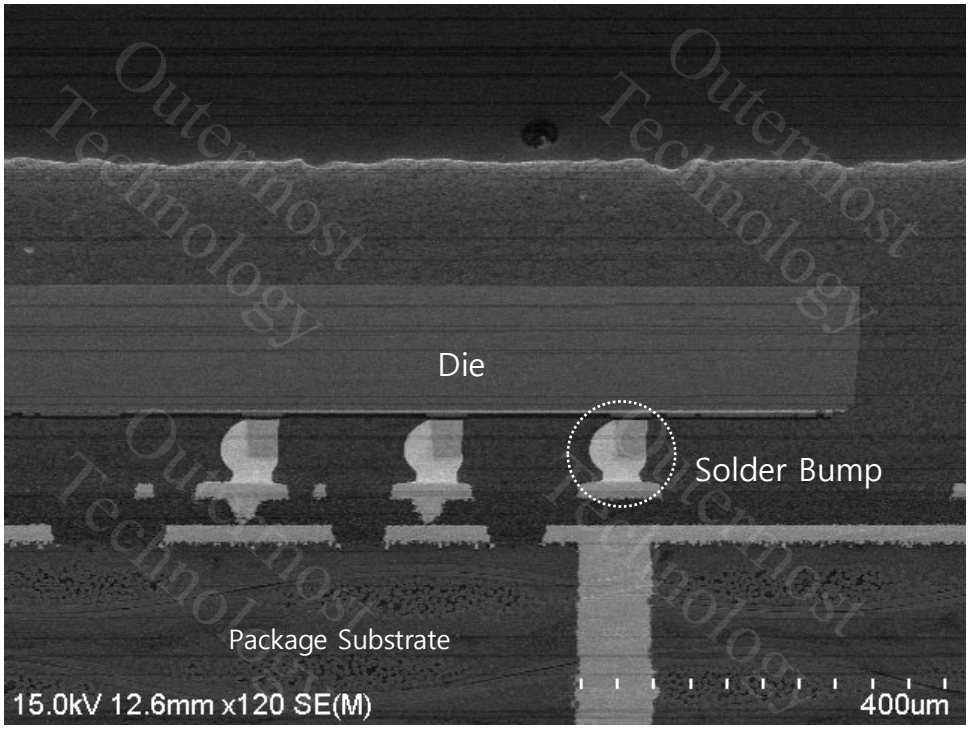

Figure 1.1.8: Connection of bump pads cross-sectional image

1.2 Die Overview

Feature	Dimension	Unit
Die Marking	XXXXXXX	-
Die Size	18.19 (4.75 x 3.83)	mm2

Figure 1.2.1: Die summary

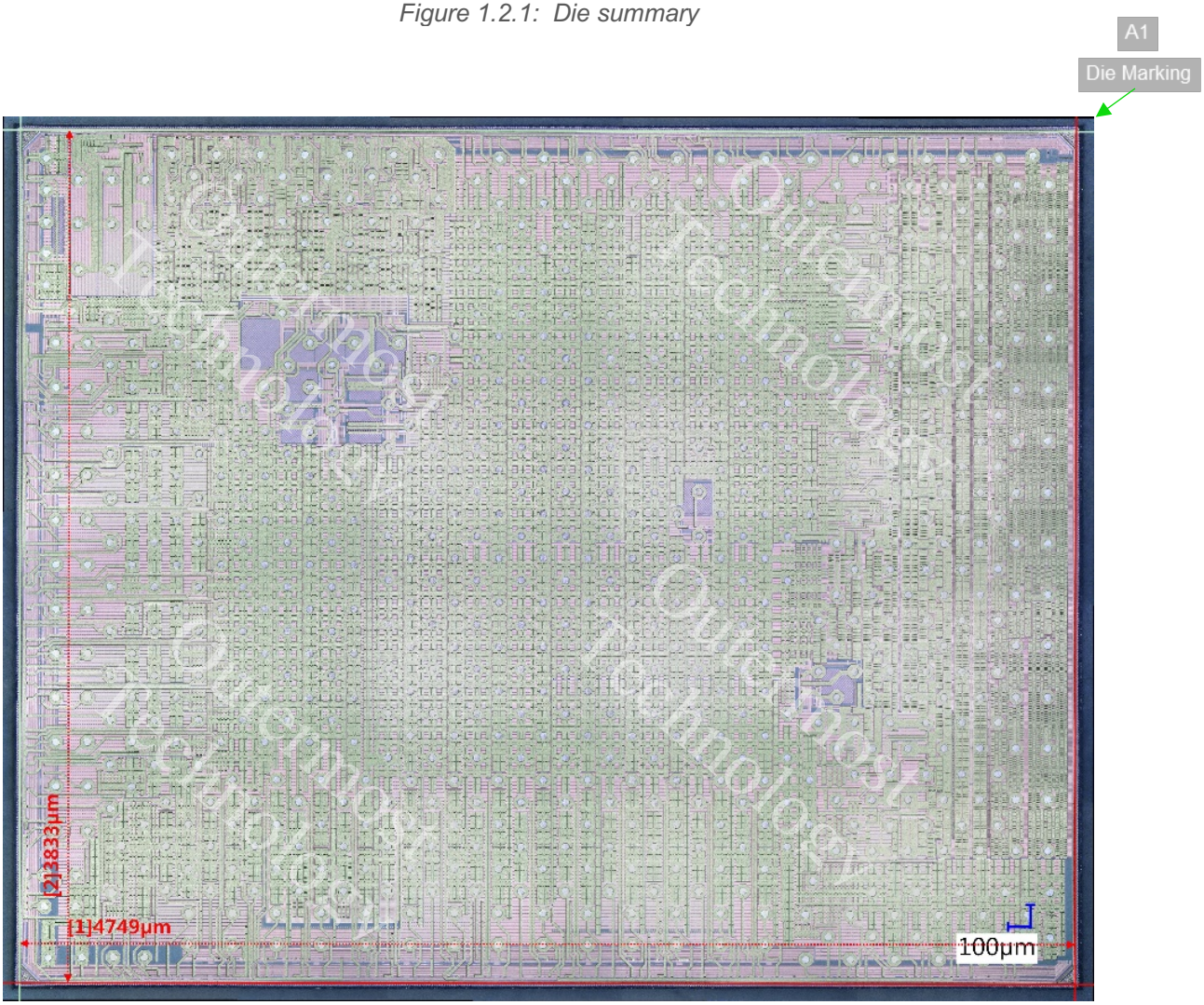

Figure 1.2.2: Size measurement of die

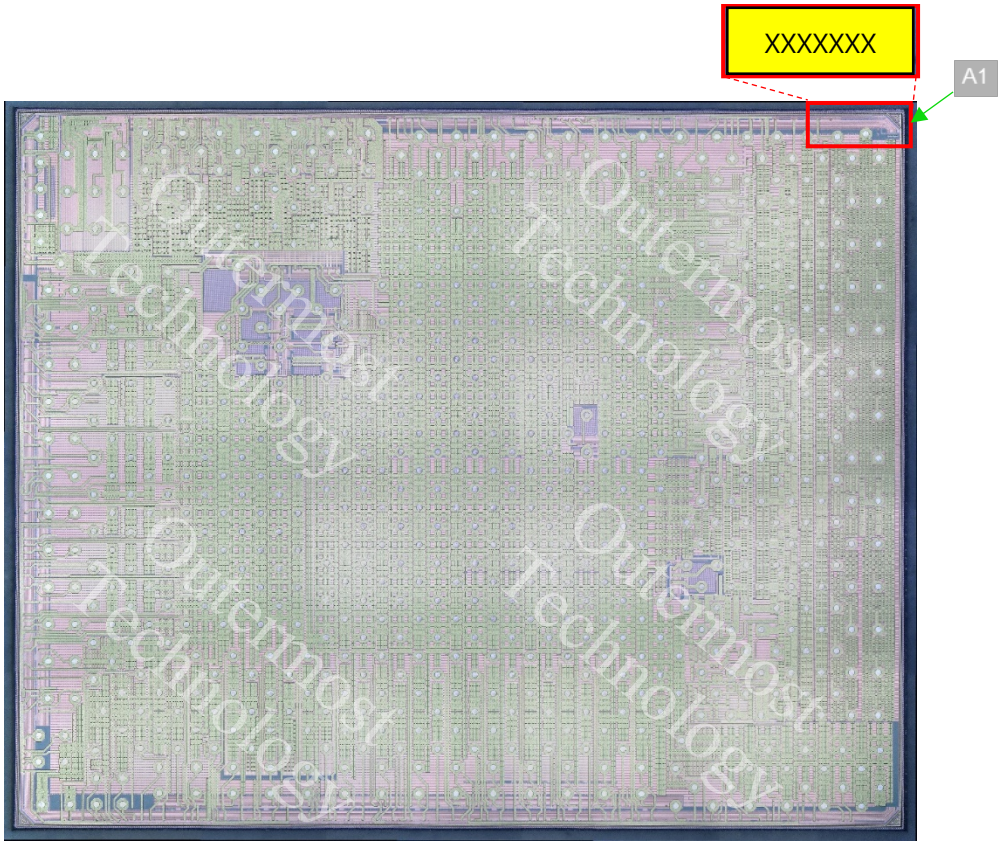

Figure 1.2.3: Die photograph & logo

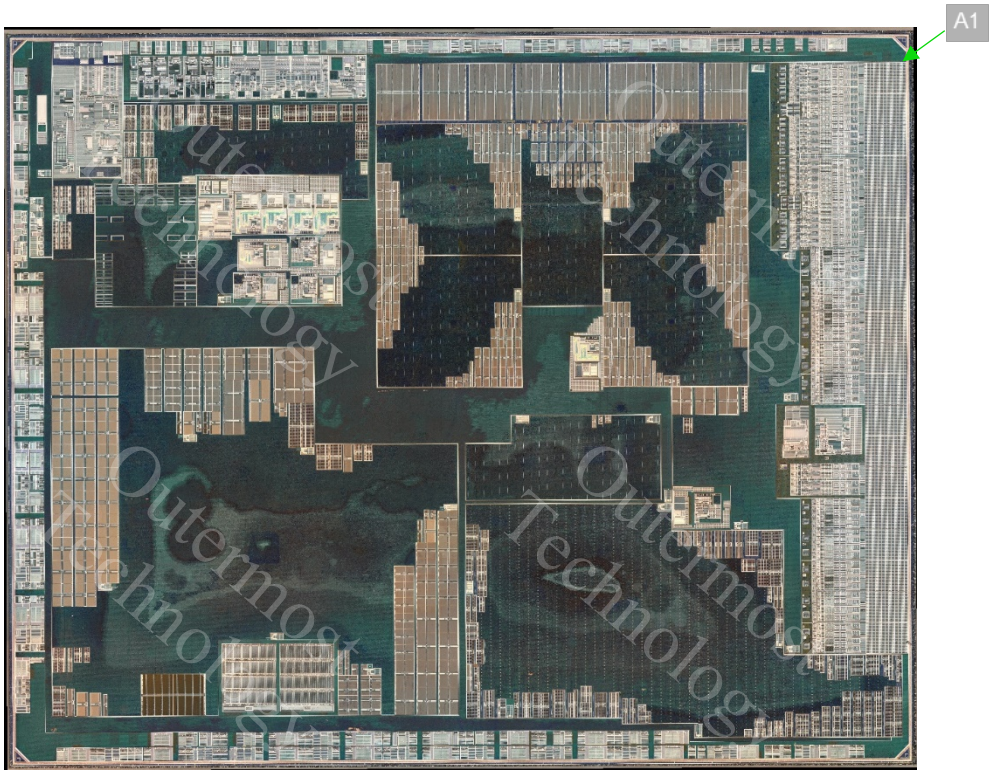

Figure 1.2.4: Die photograph with the sample delayered to substrate (fins level)

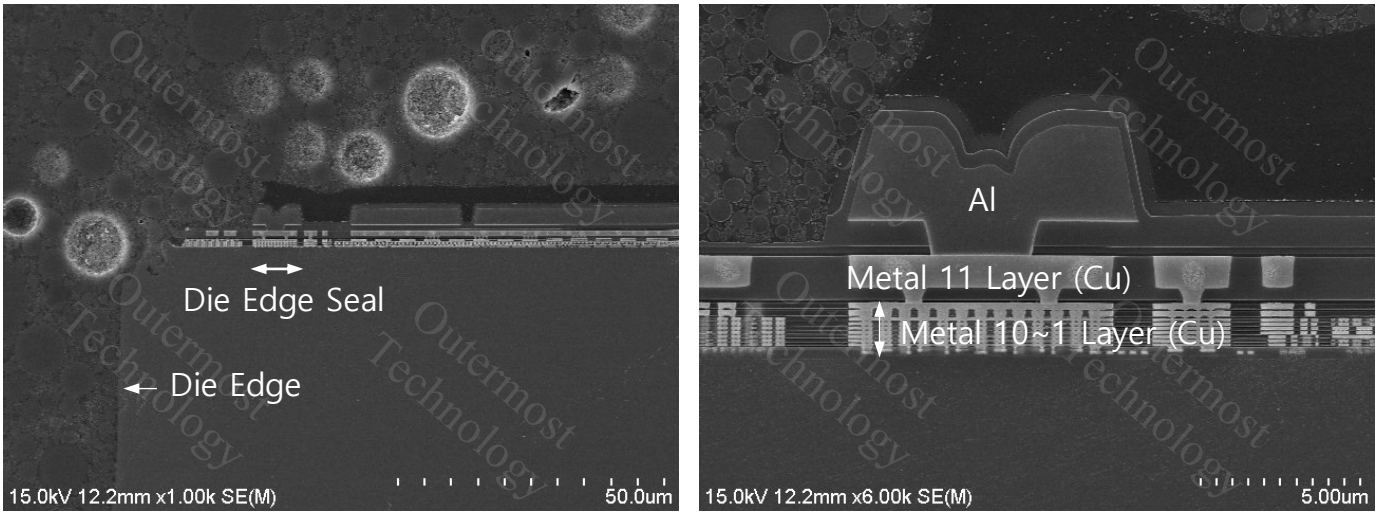

Figure 1.2.5: Edge of scribe lane and die edge seal cross-sectional image

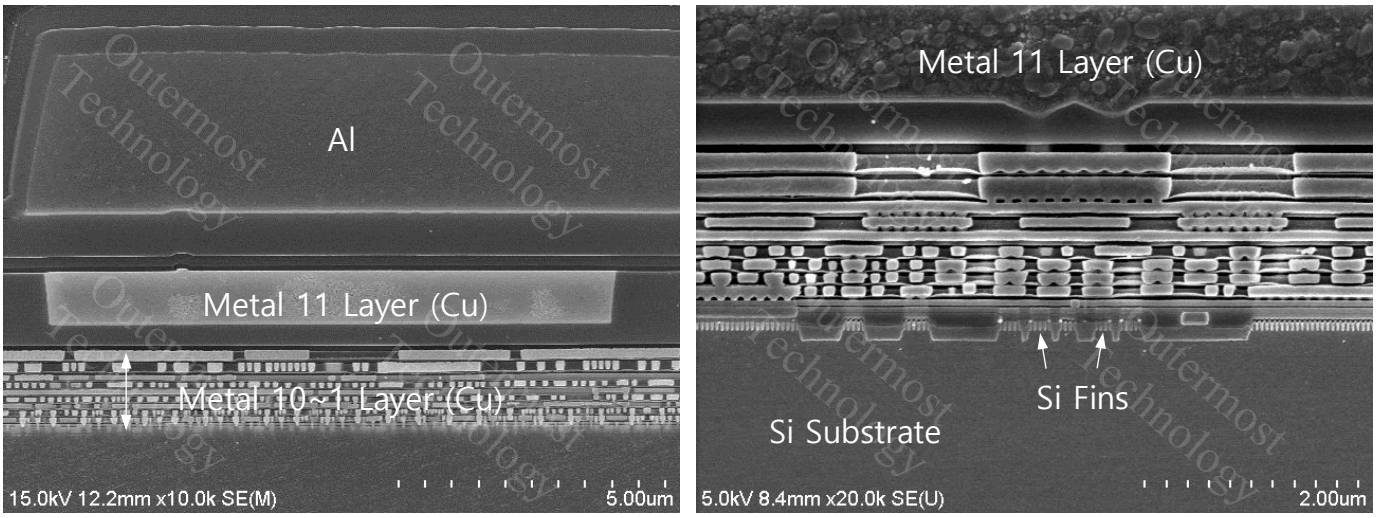

Figure 1.2.6: Process overview cross-sectional image

1.3 Bump Information

Feature	Dimension	Unit
Bump count	730	EA
Bump pad size	33.2	um
Bump pad pitch	140.5	um

Figure 1.3.1: Bump pads summary

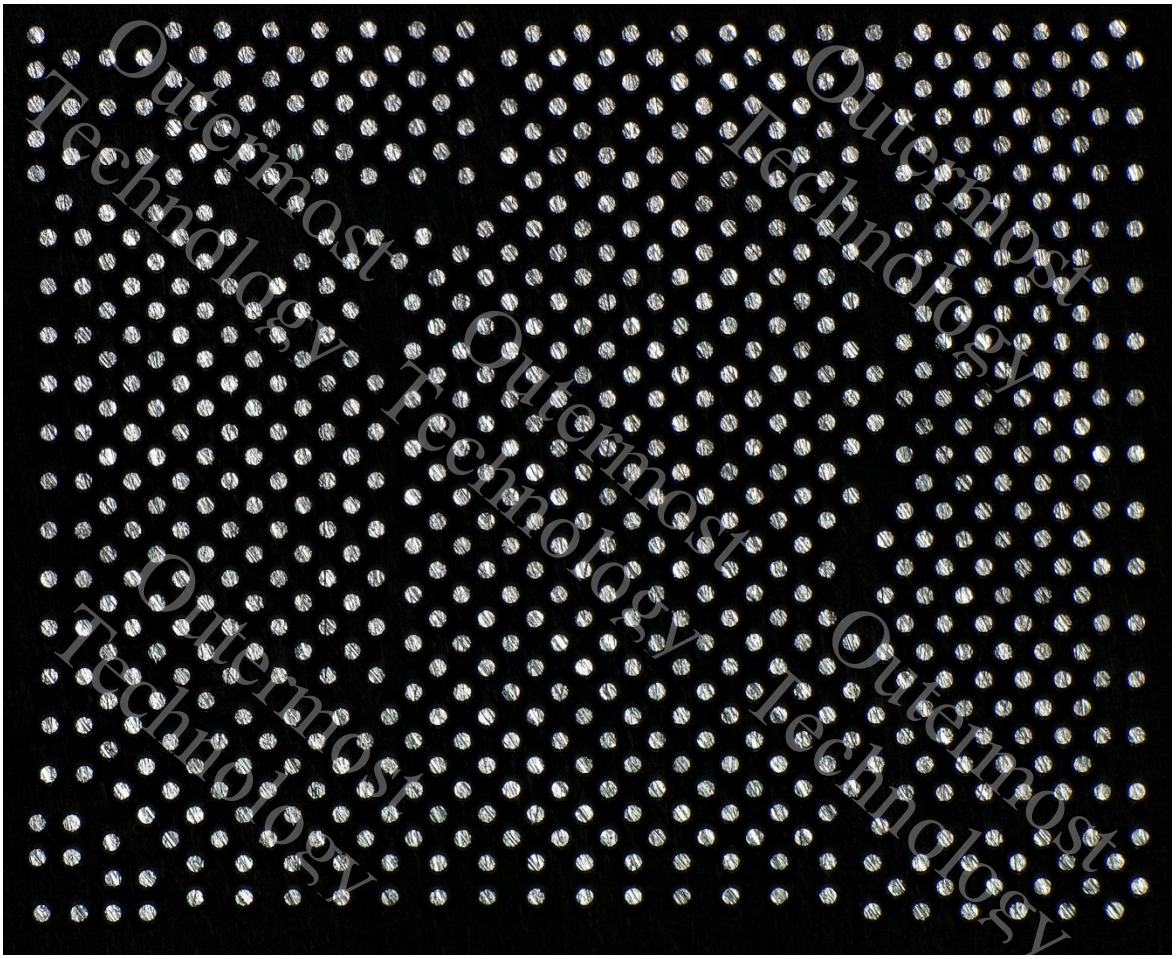

Figure 1.3.2: Bump pads image

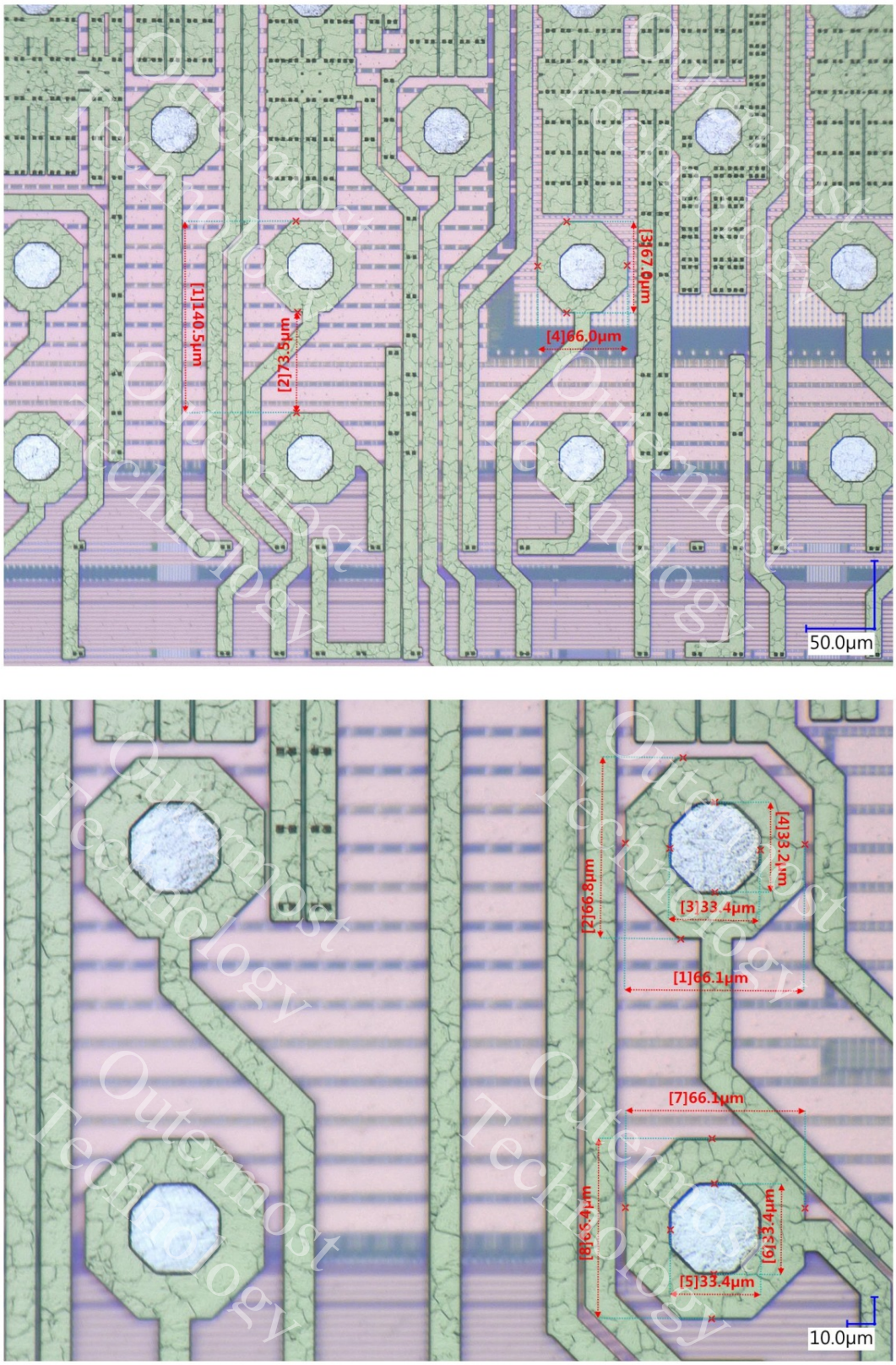

Figure 1.3.3: Bump pads image

2.0 Process Overview

2.1 Metallization

- Process : 12Metal 1Gate (ML1 ~ ML11 Cu, 1 Al)

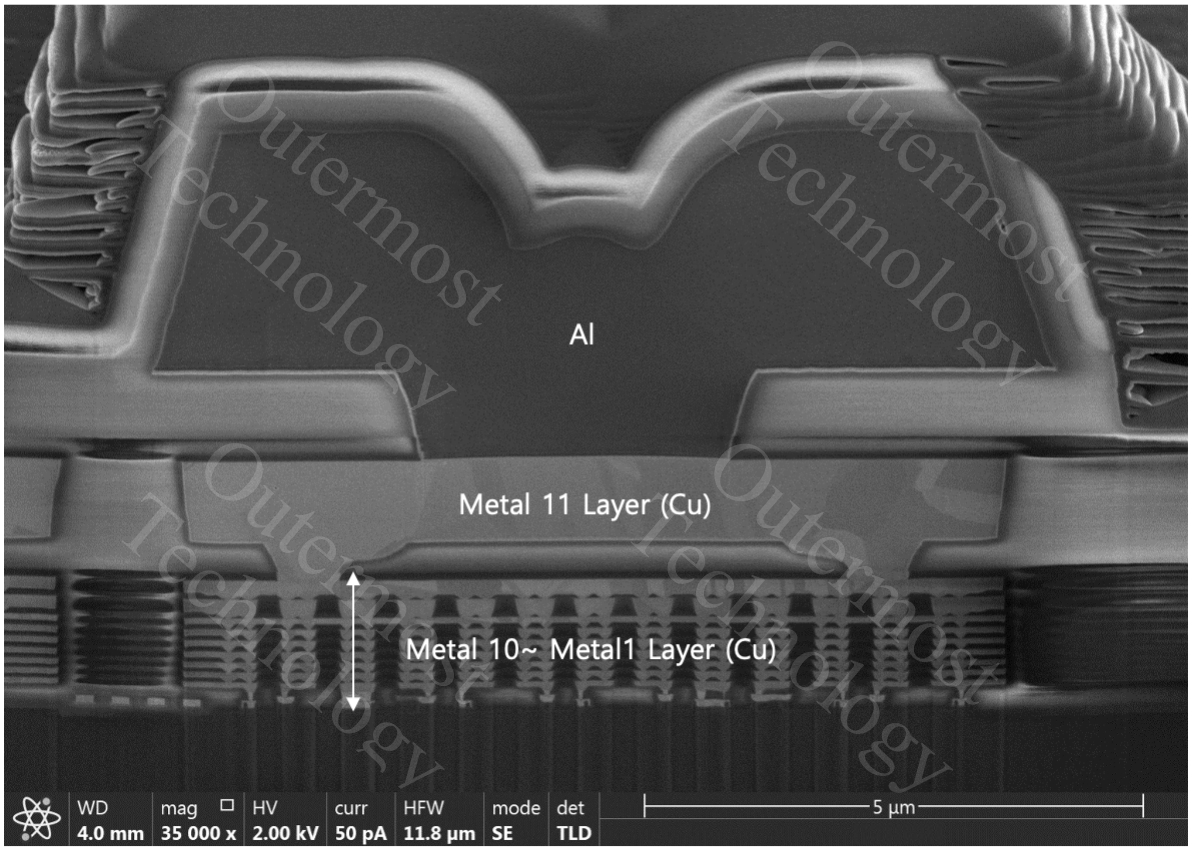

Figure 2.1.1: Metal levels 1 through 12, FIB cross sectional image

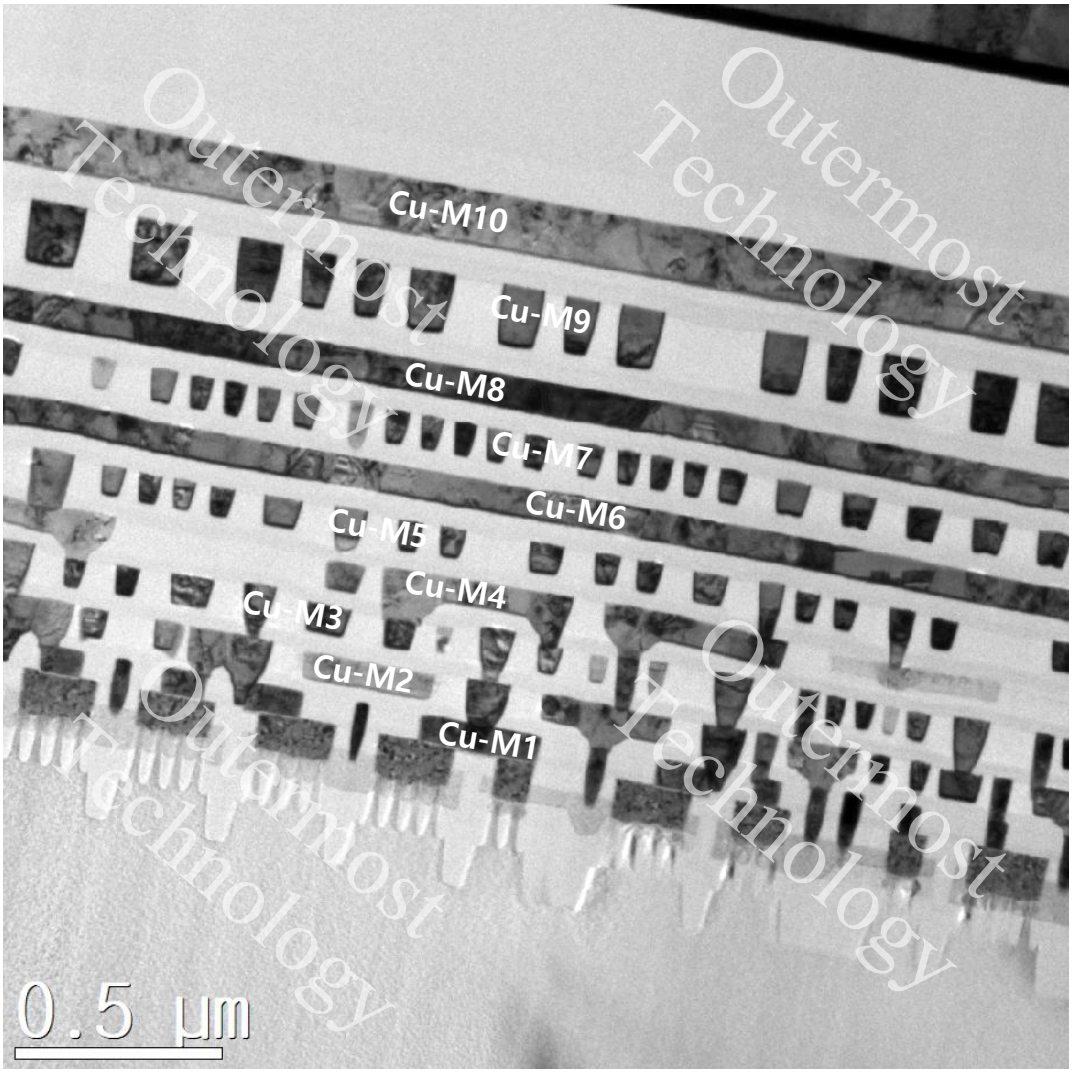

Figure 2.1.2: Metal levels 1 through 10, TEM cross sectional image

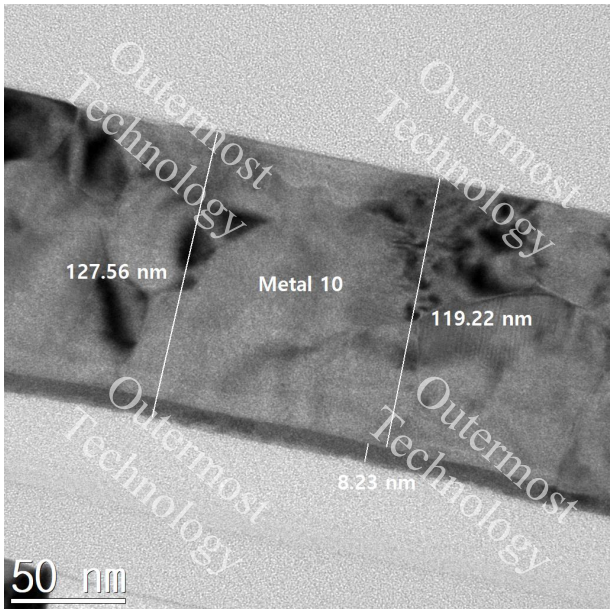

Figure 2.1.3 Metal-10, TEM cross sectional image

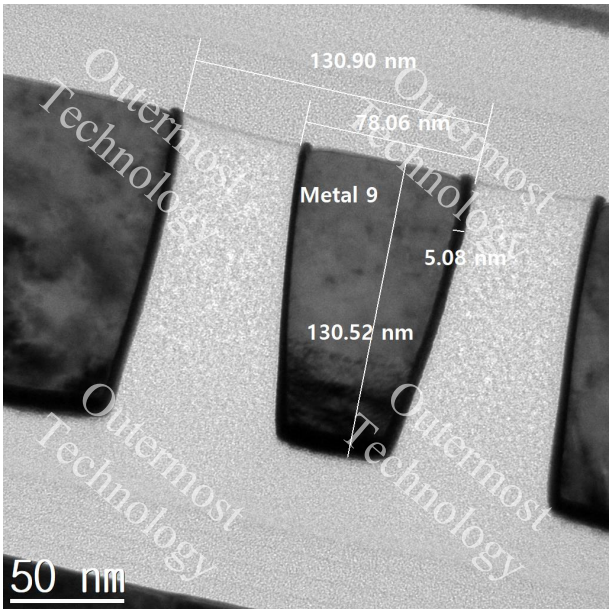

Figure 2.1.4 Metal-9, TEM cross sectional image

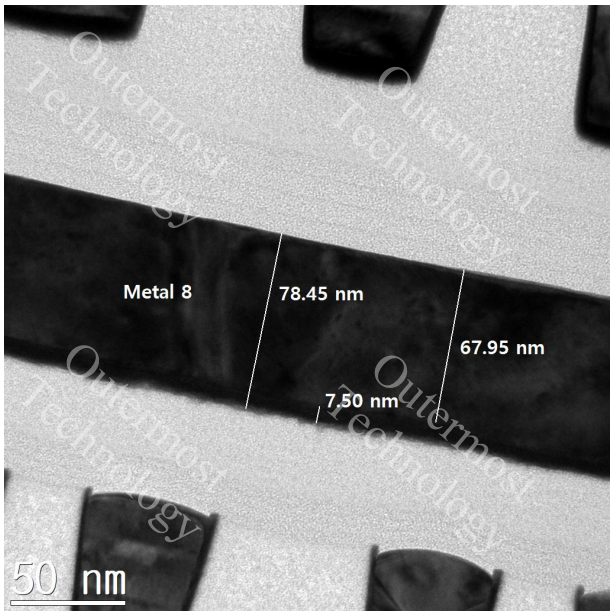

Figure 2.1.5 Metal-8, TEM cross sectional image

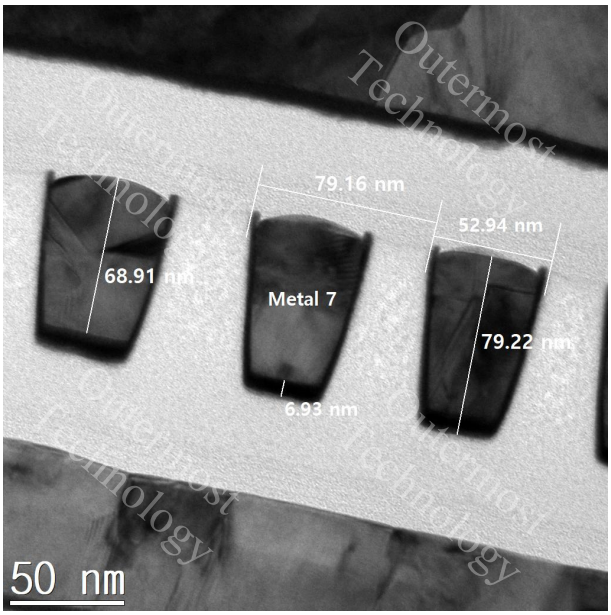

Figure 2.1.6 Metal-7, TEM cross sectional image

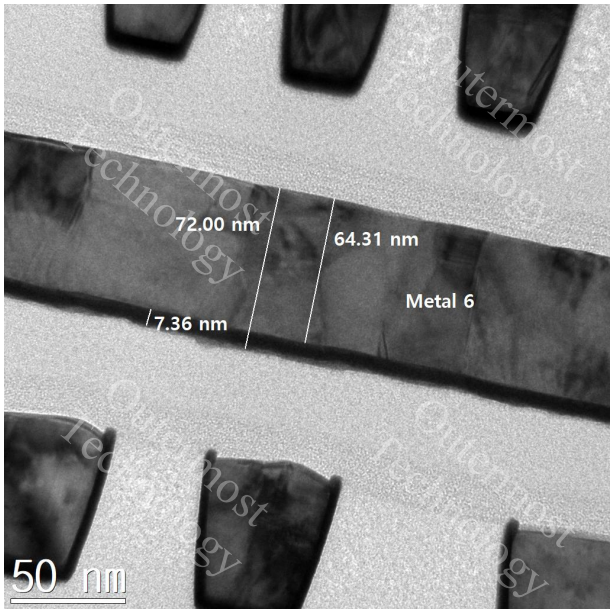

Figure 2.1.7 Metal-6, TEM cross sectional image

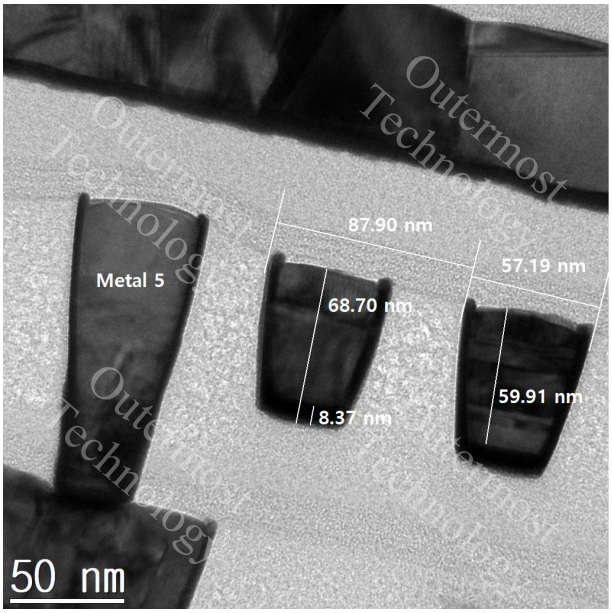

Figure 2.1.8 Metal-5, TEM cross sectional image

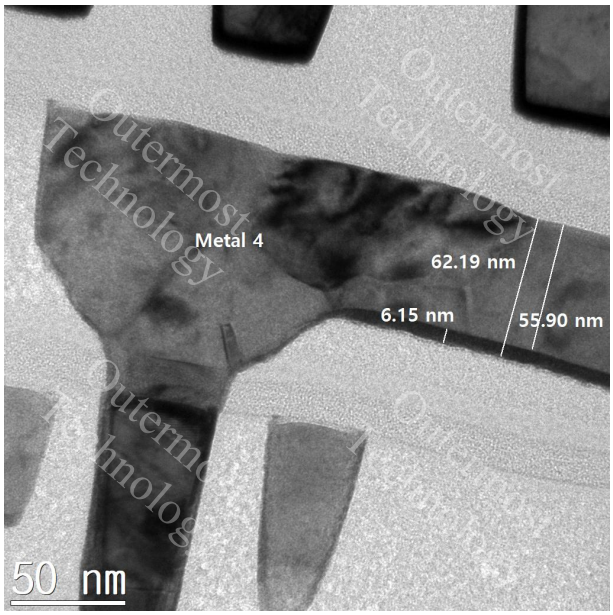

Figure 2.1.9 Metal-4, TEM cross sectional image

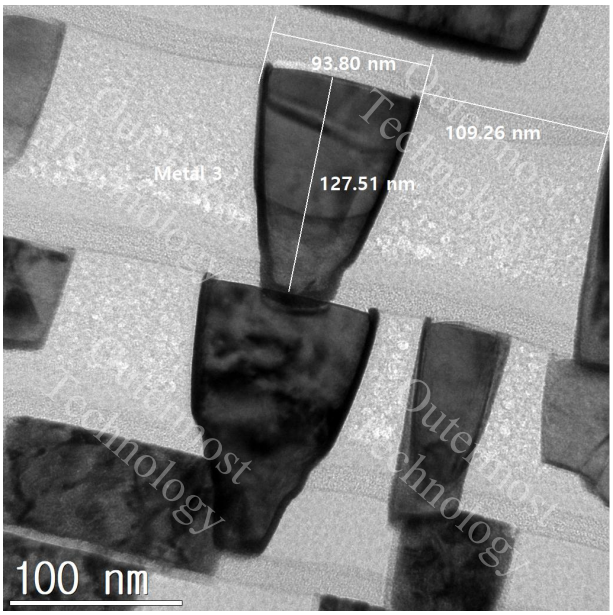

Figure 2.1.10 Metal-3, TEM cross sectional image

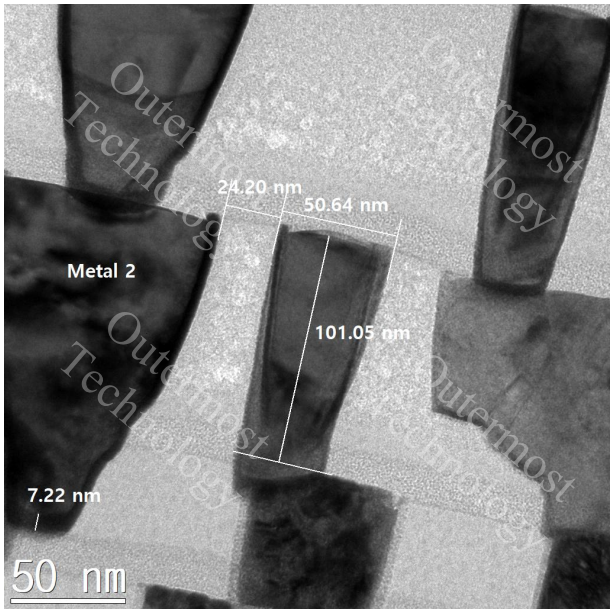

Figure 2.1.11 Metal-2, TEM cross sectional image

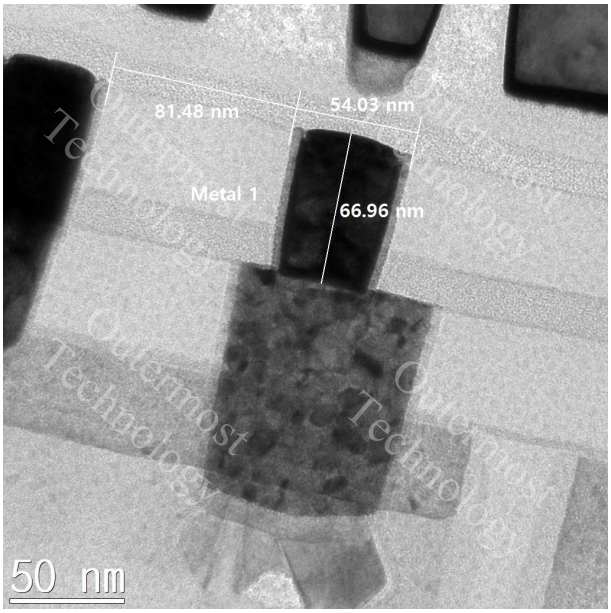

Figure 2.1.12 Metal-1, TEM cross sectional image

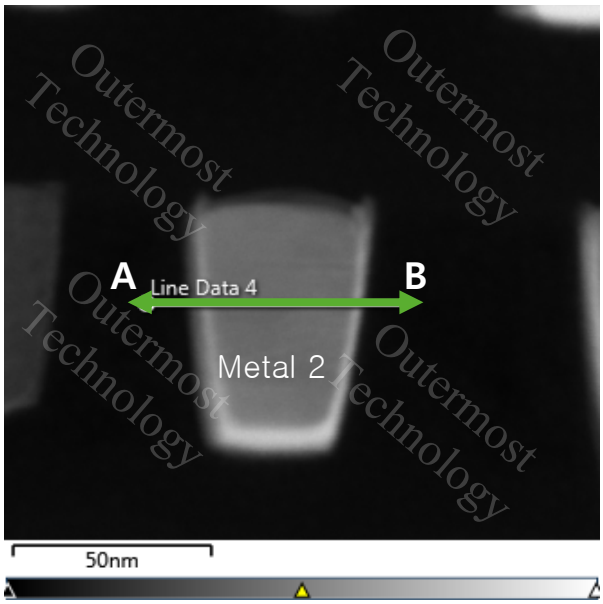

Figure 2.1.13 TEM-EDS analysis locations on metal 2, TEM cross sectional image

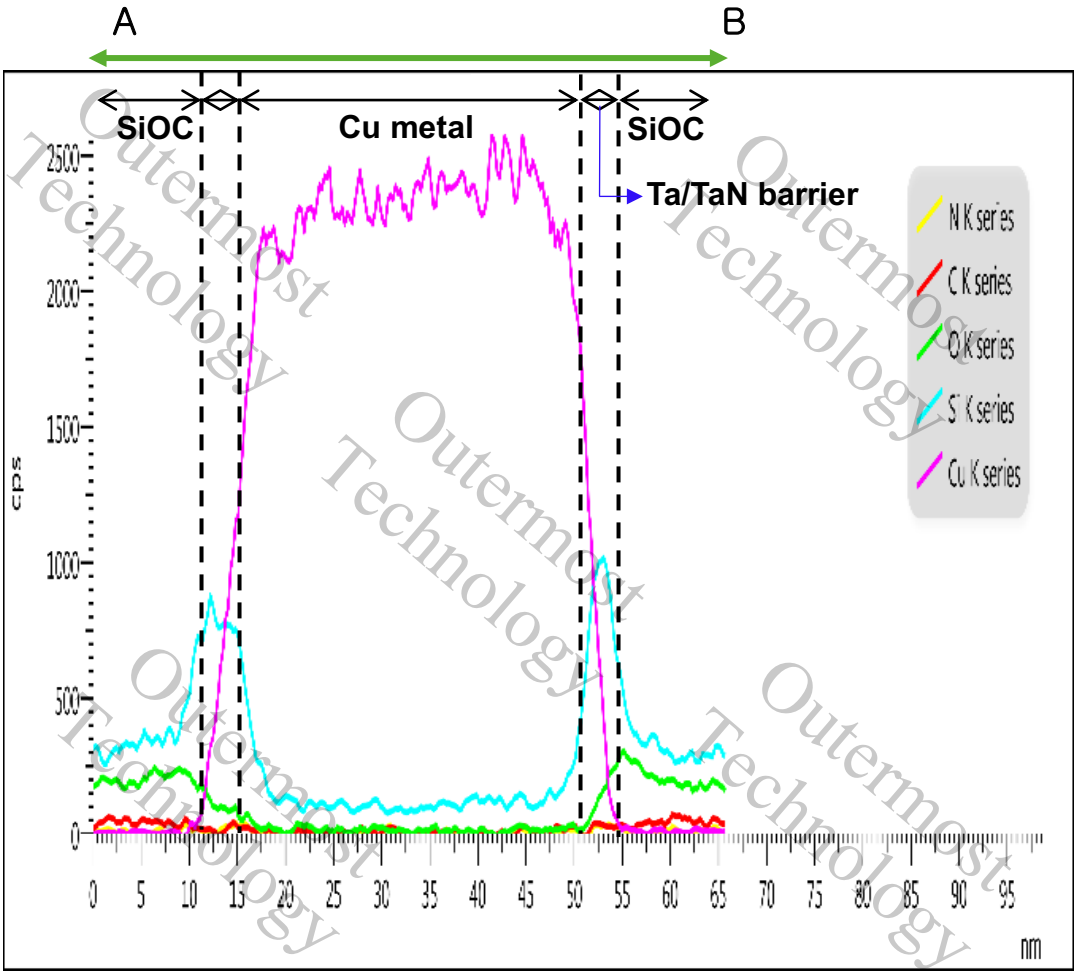

Figure 2.1.14 TEM-EDS profile from Figure 2.1.13

2.2 IMD & ILD Overview

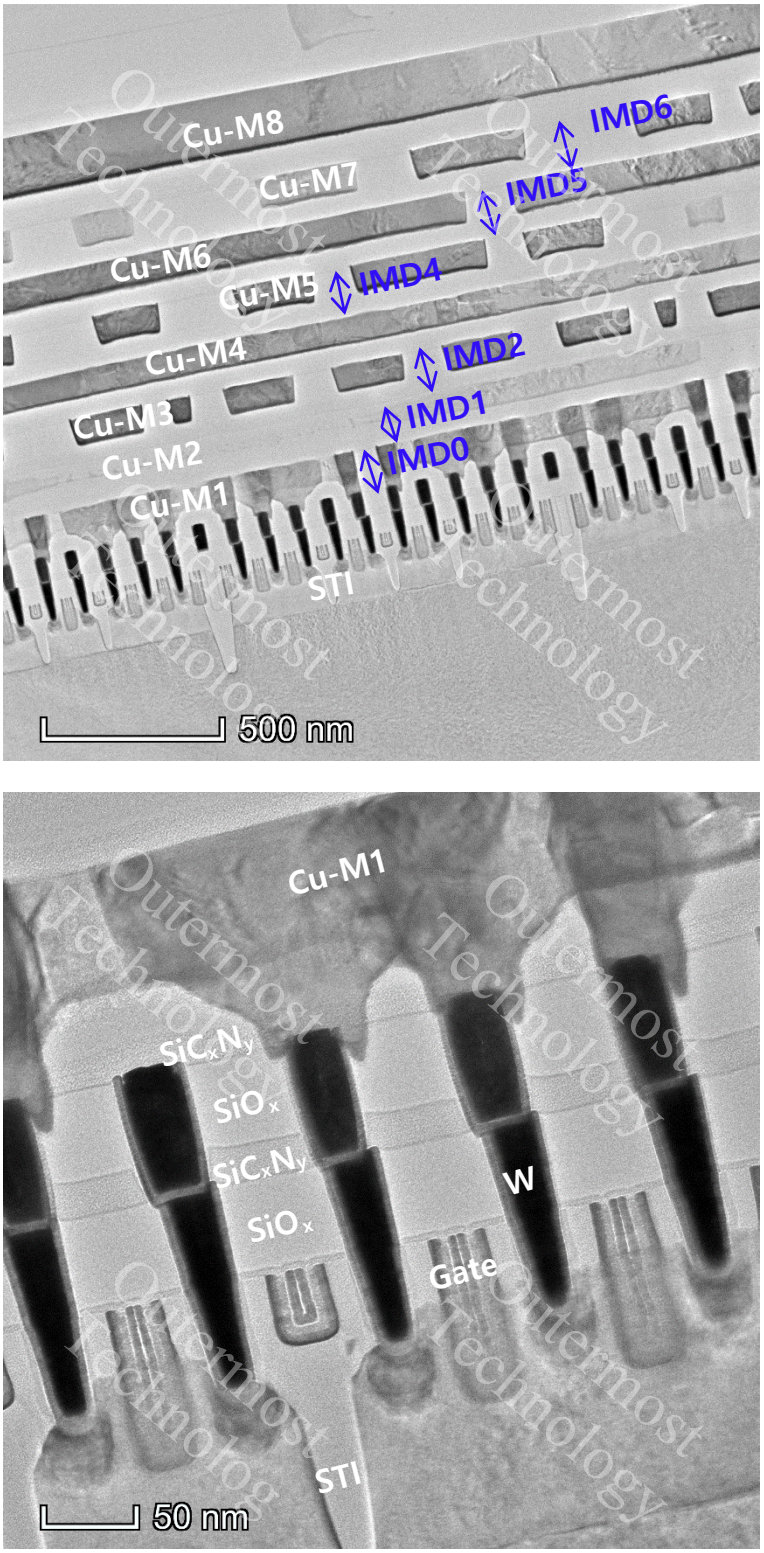

Figure 2.2.1 IMD & ILD layer stack composition, TEM cross sectional image

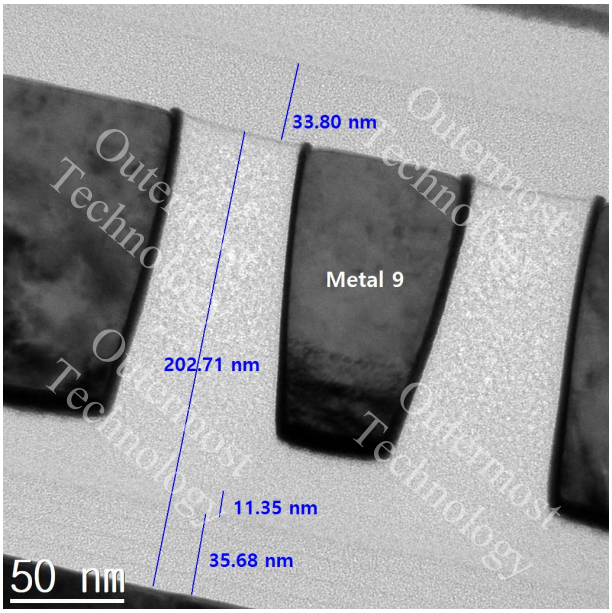

Figure 2.2.2 IMD-8, TEM cross sectional image

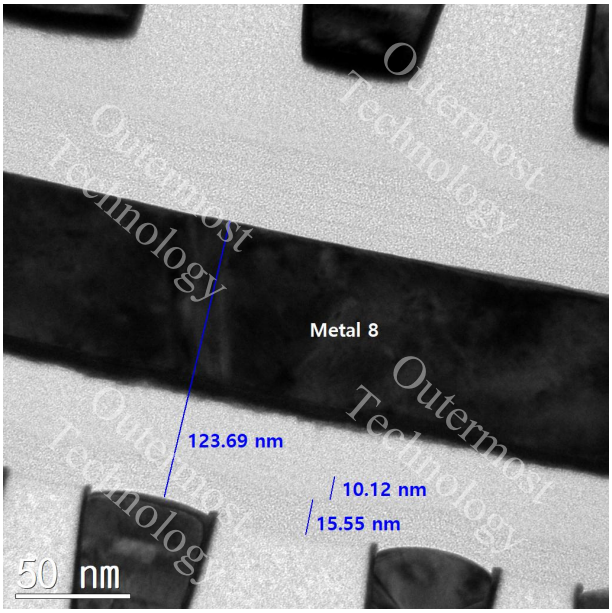

Figure 2.2.3 IMD-7, TEM cross sectional image

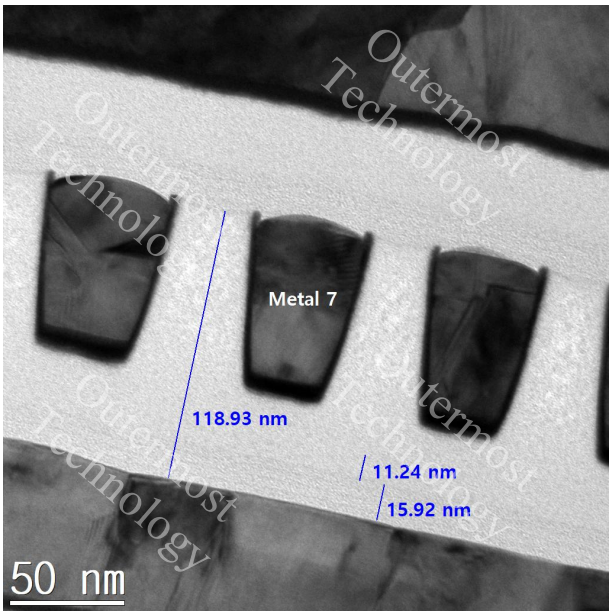

Figure 2.2.4 IMD-6, TEM cross sectional image

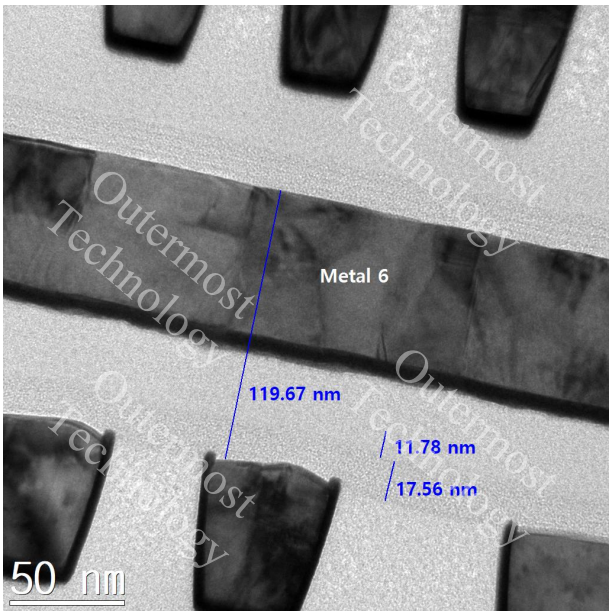

Figure 2.2.5 IMD-5, TEM cross sectional image

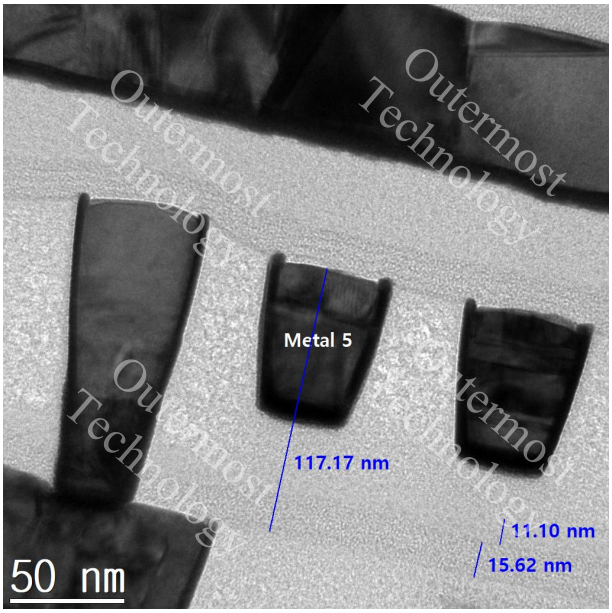

Figure 2.2.6 IMD-4, TEM cross sectional image

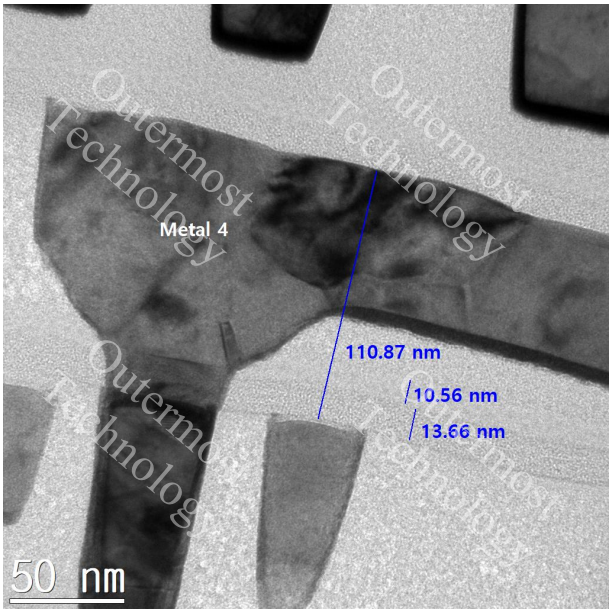

Figure 2.2.7 IMD-3, TEM cross sectional image

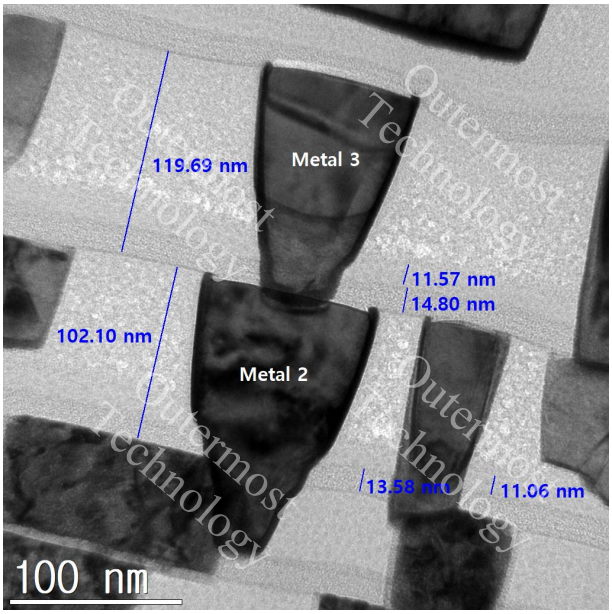

Figure 2.2.8 IMD-2 & 1, TEM cross sectional image

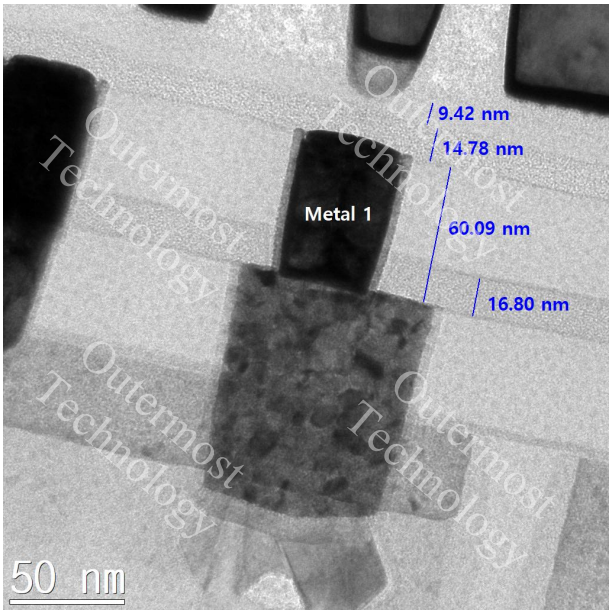

Figure 2.2.9 IMD-0, TEM cross sectional image

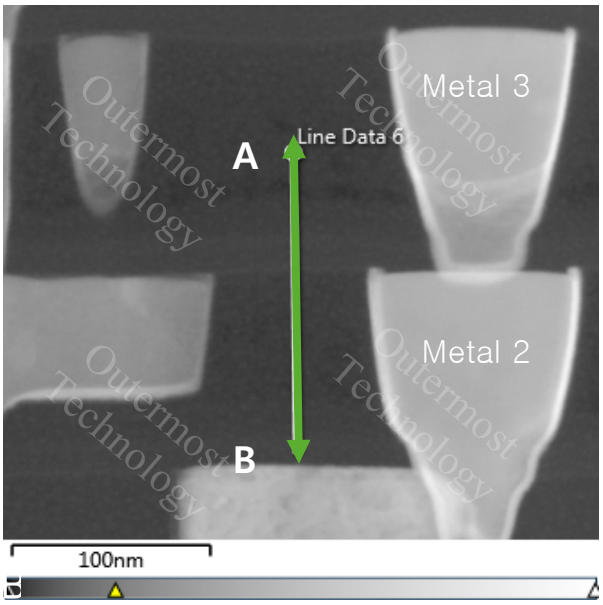

Figure 2.2.10 TEM-EDS analysis locations on IMD, TEM cross sectional image

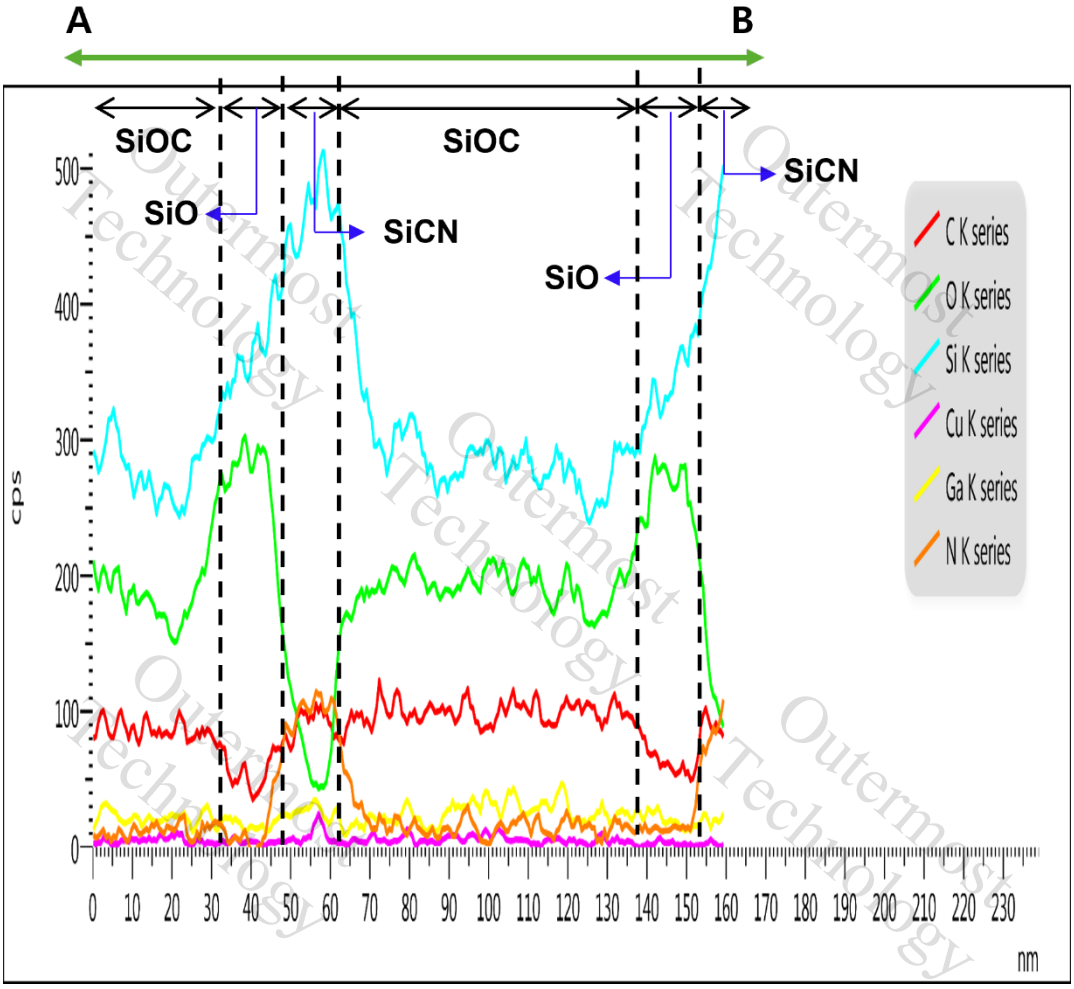

Figure 2.2.11 TEM-EDS profile from Figure 2.2.10

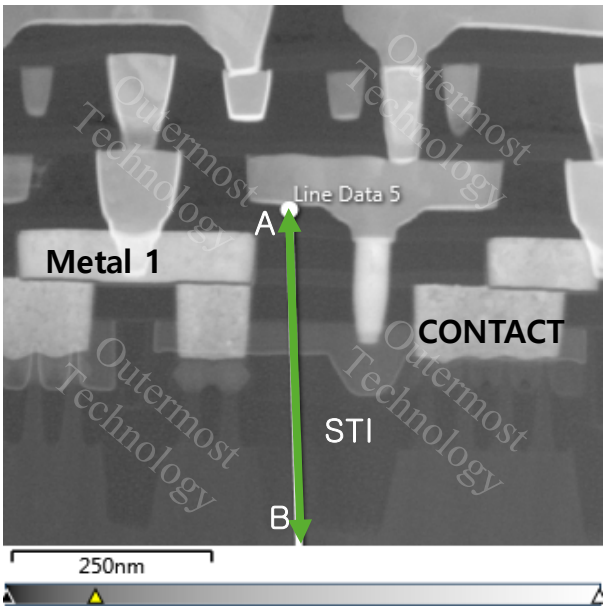

Figure 2.2.12 TEM-EDS Analysis locations on ILD, TEM cross sectional image

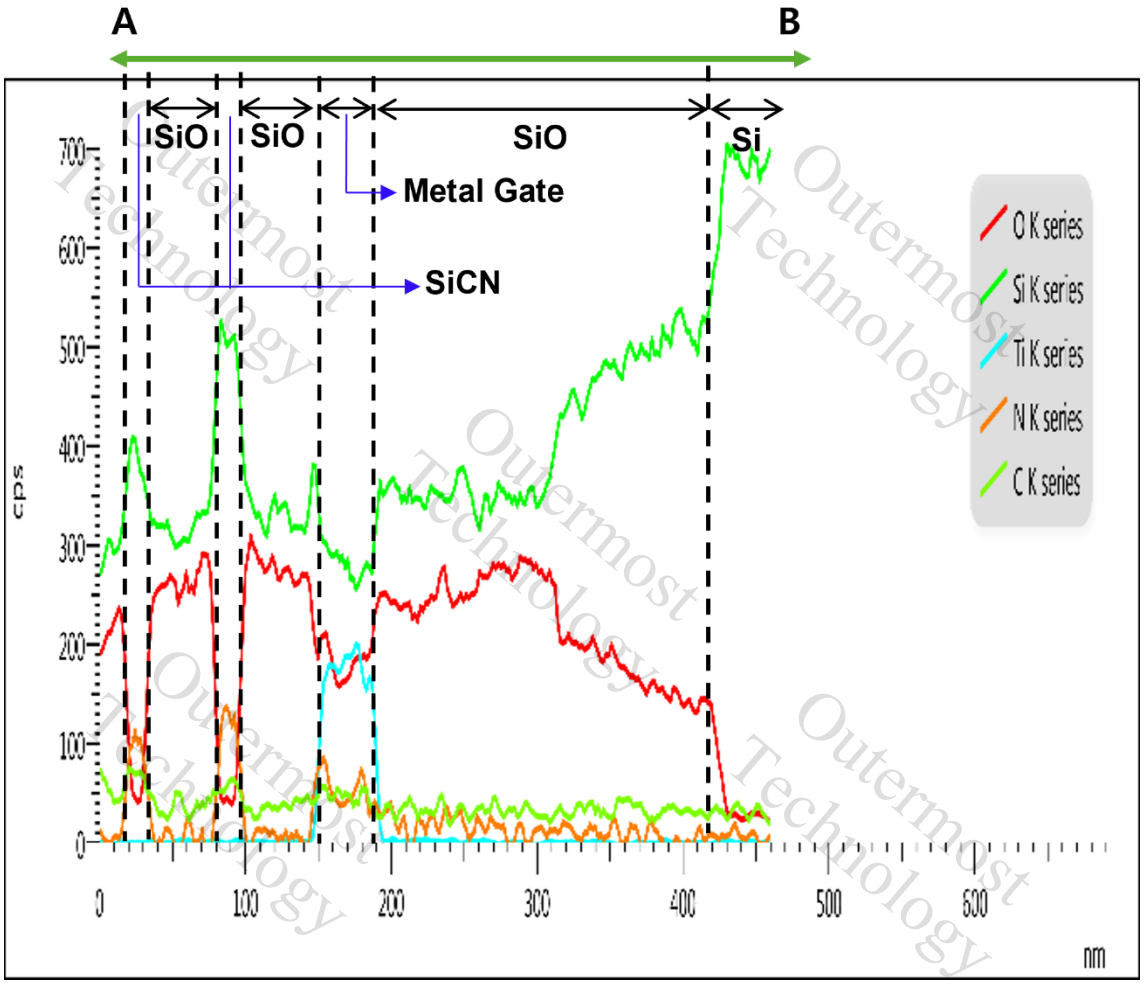

Figure 2.2.13 TEM-EDS profile from Figure 2.2.12

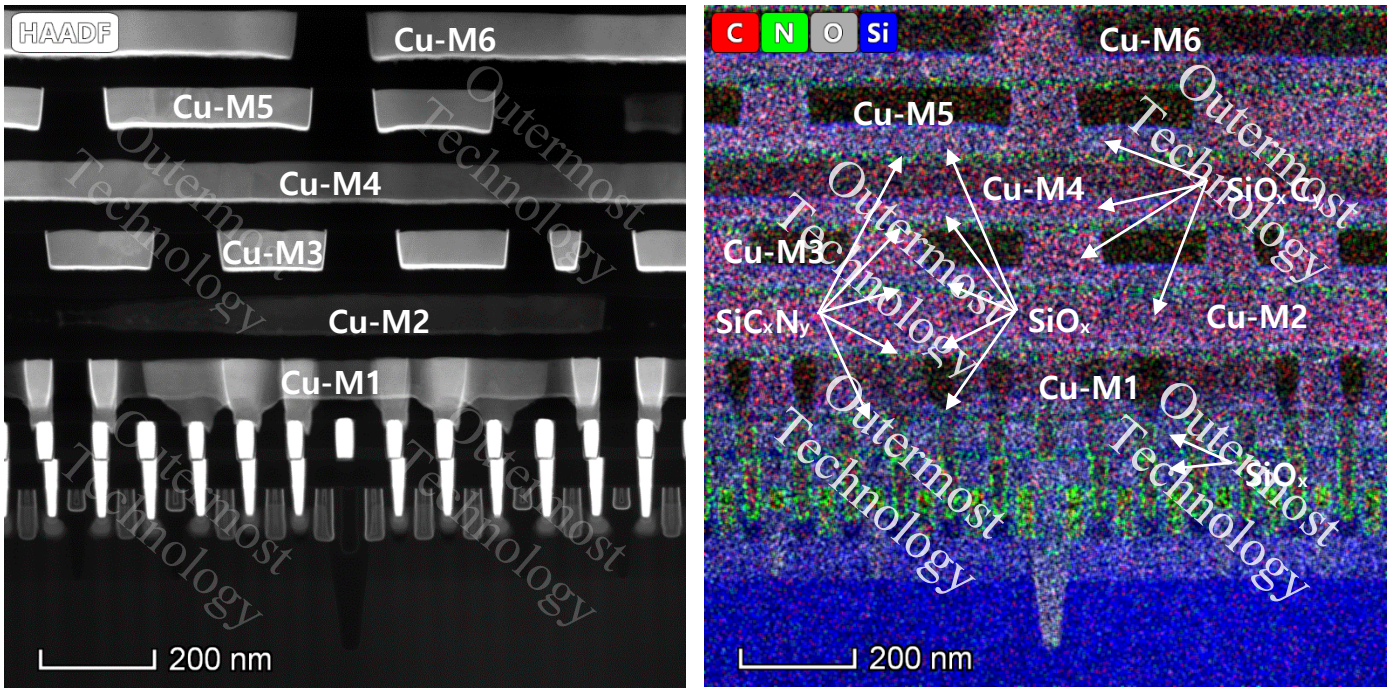

Figure 2.2.14 EDS mapping results for about IMD & ILD layer stack composition

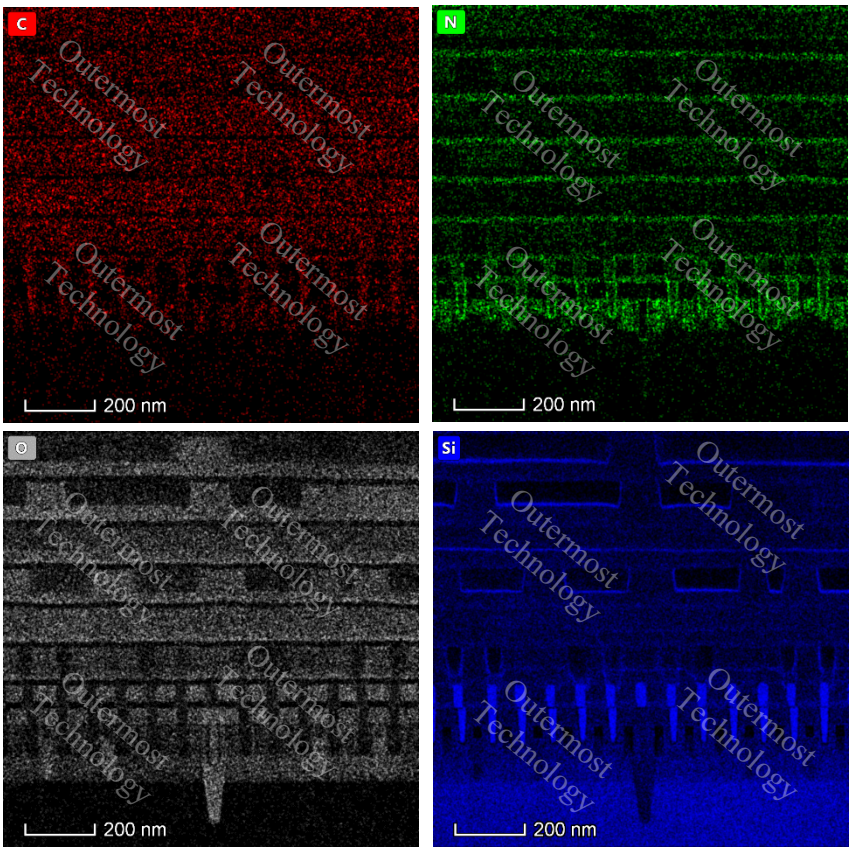

Figure 2.2.15 EDS mapping data for each element (C, N, O, Si)

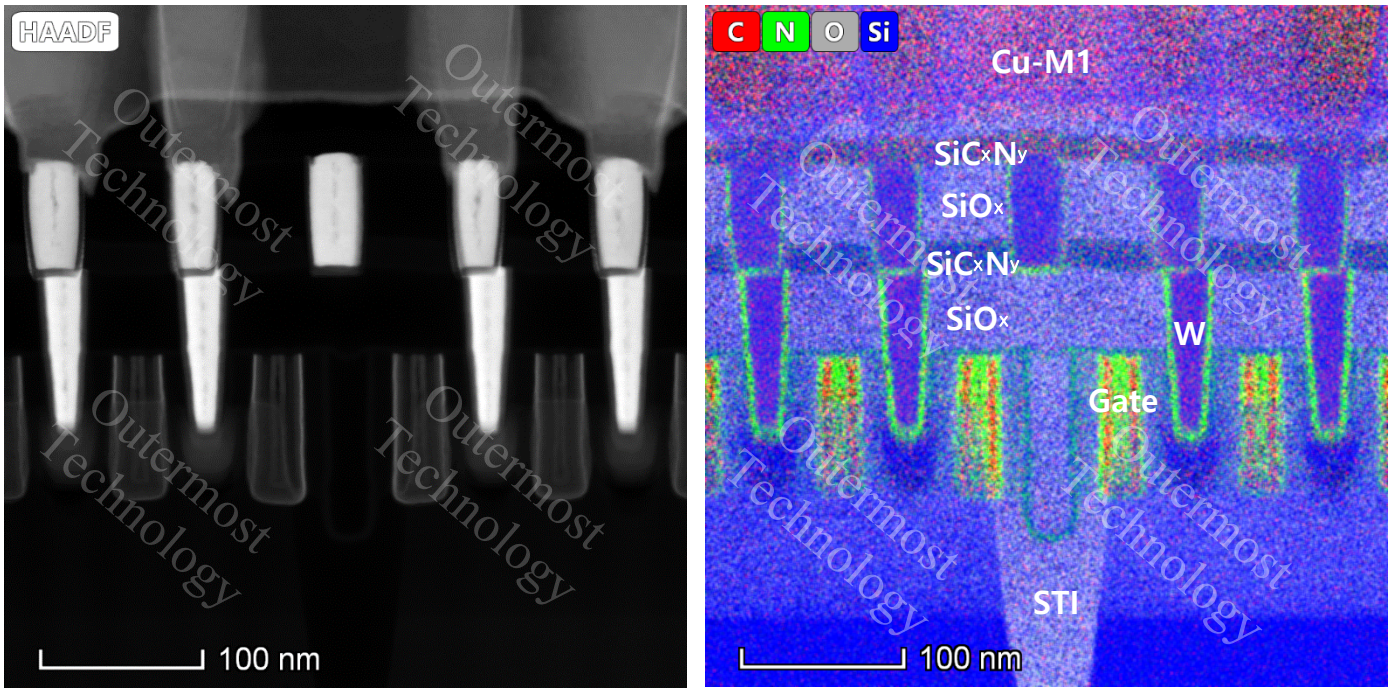

Figure 2.2.16 EDS mapping results for about ILD layer

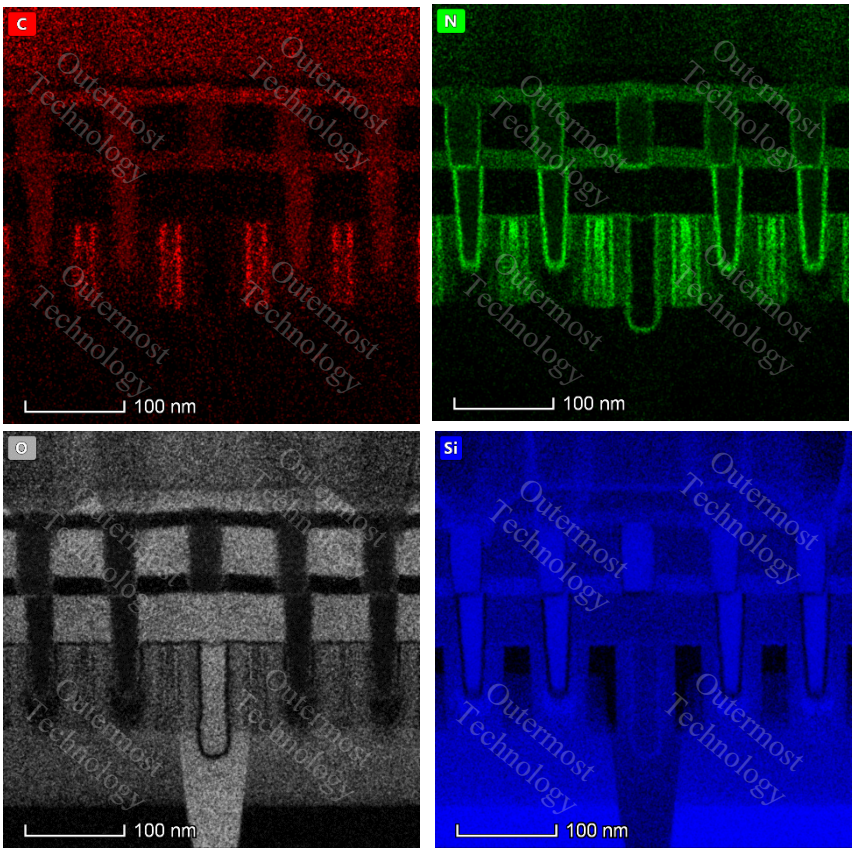

Figure 2.2.17 EDS mapping data for each element (C, N, O, Si)

2.3 Isolation and Fins

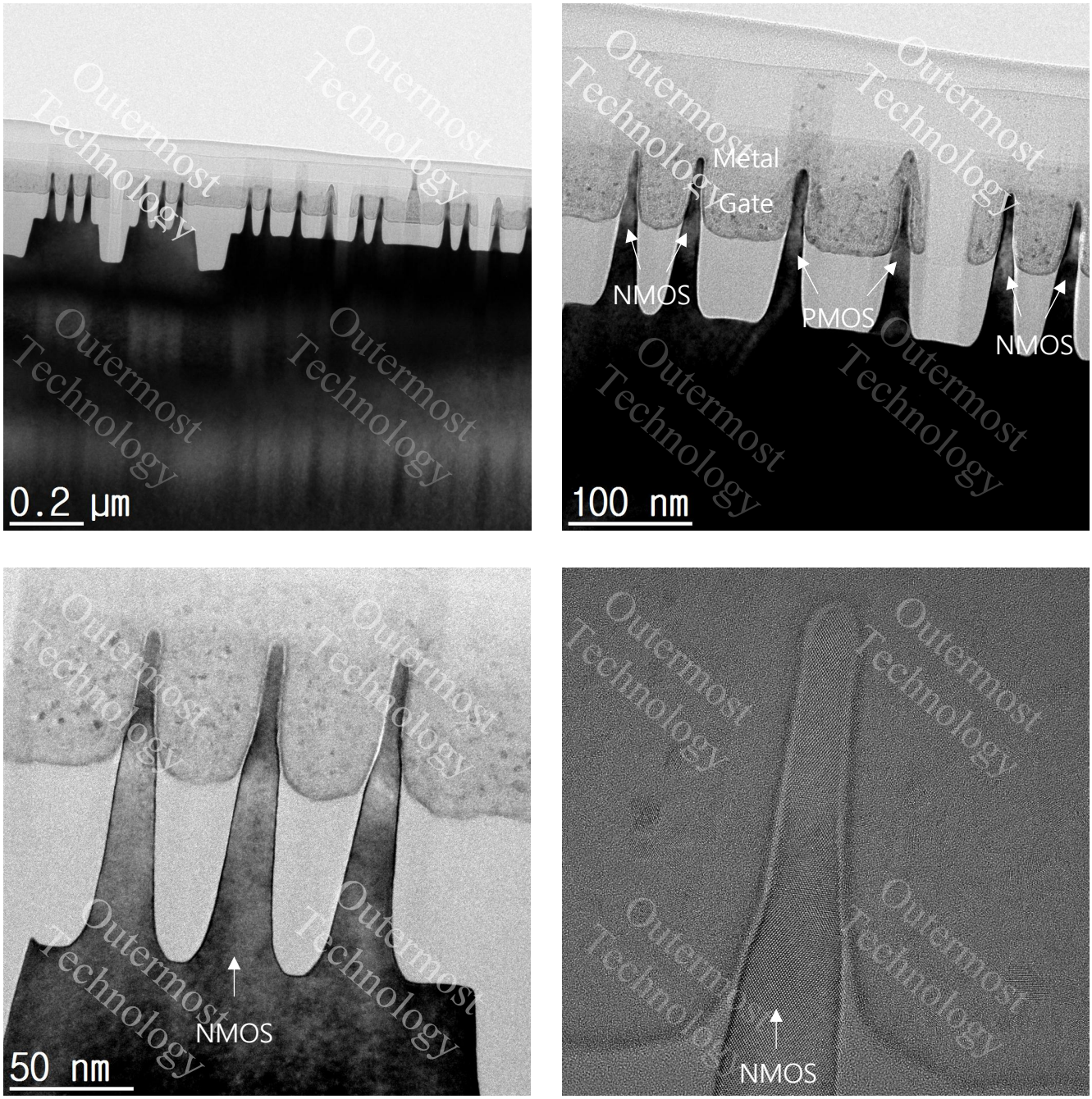

Figure 2.3.1 Overview of Si fins along gate direction, TEM cross-sectional image

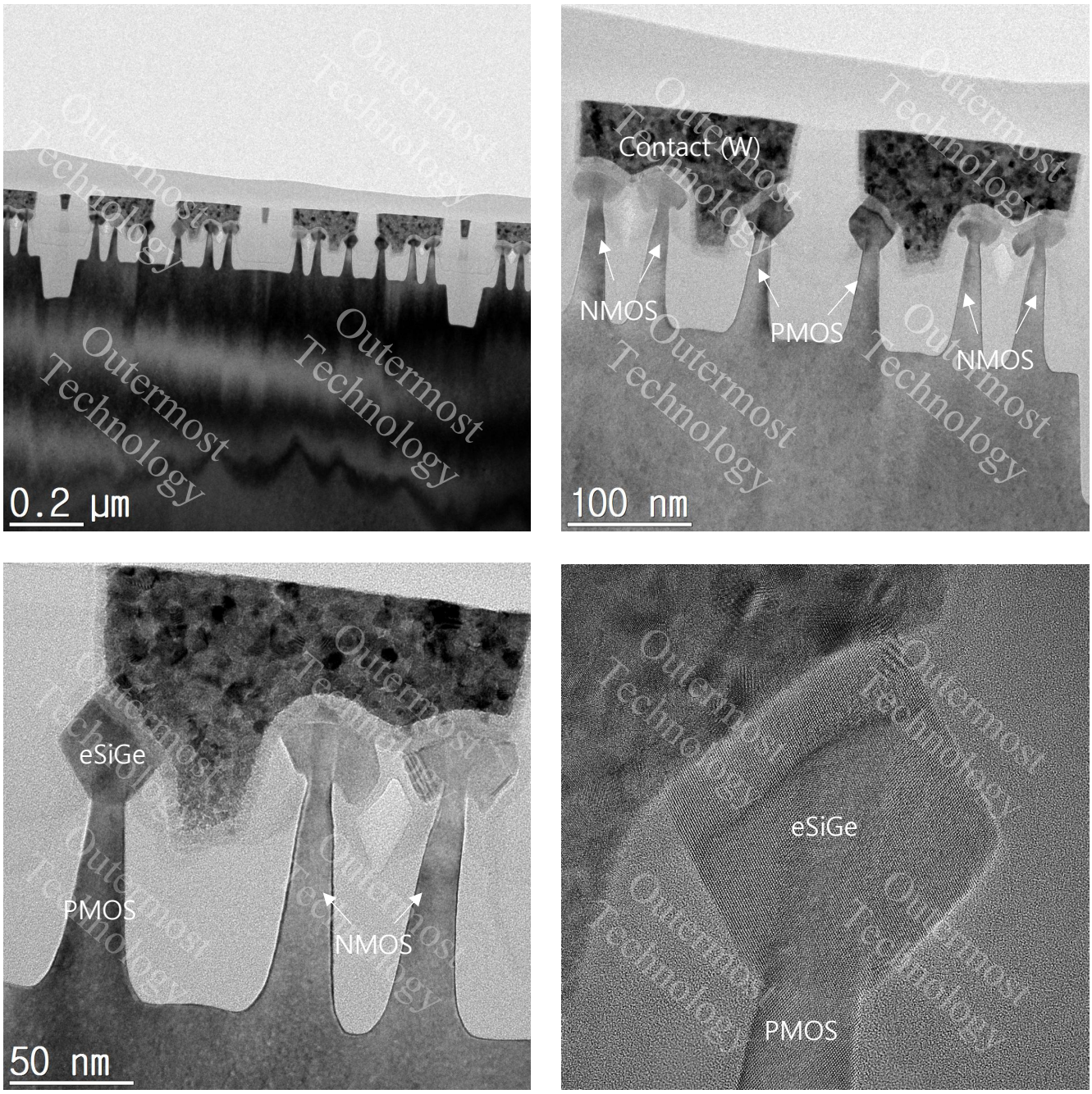

Figure 2.3.2 Overview of Si fins along gate direction, TEM cross-sectional image

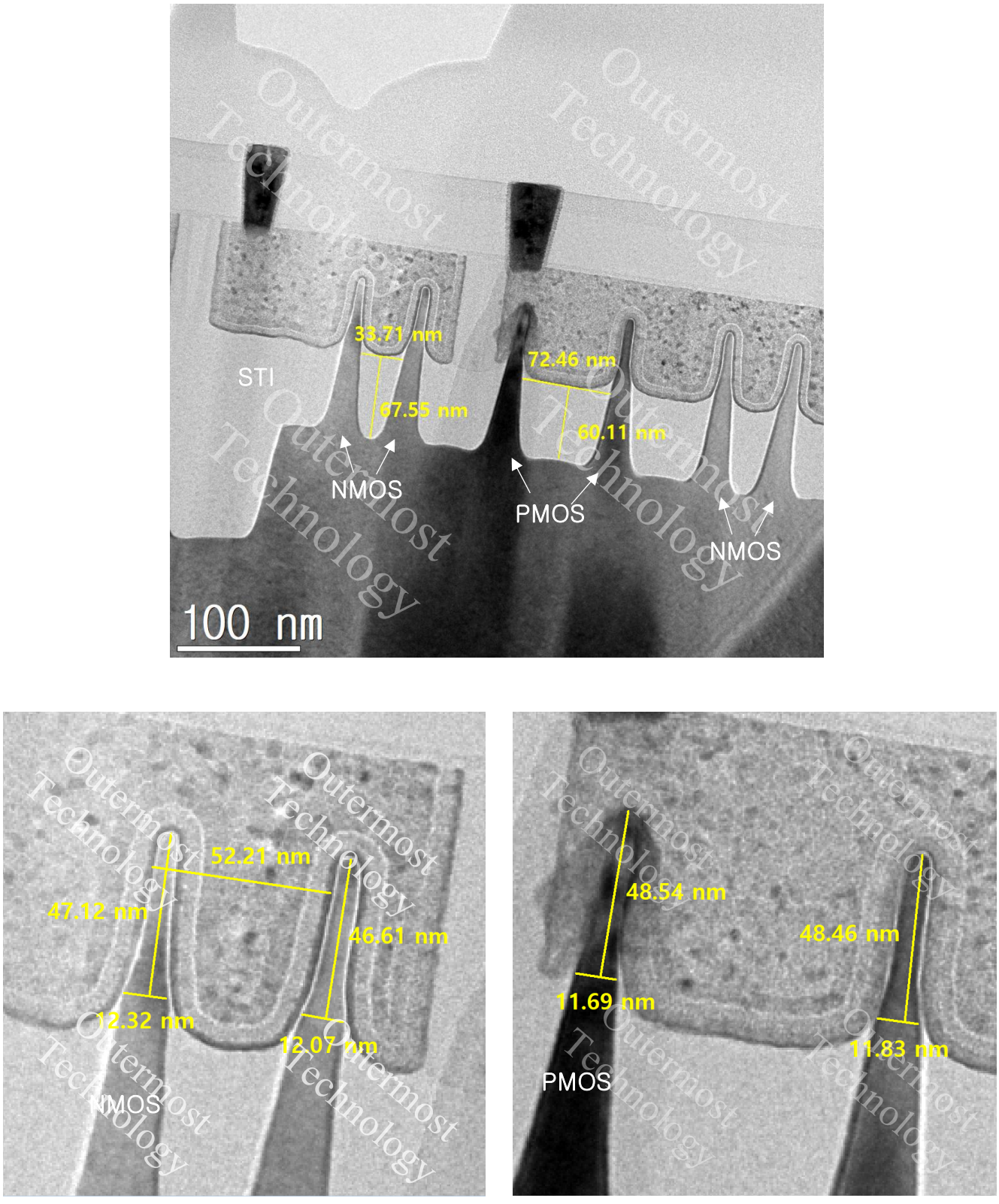

Figure 2.3.3 Si fins over STI, TEM cross-sectional image

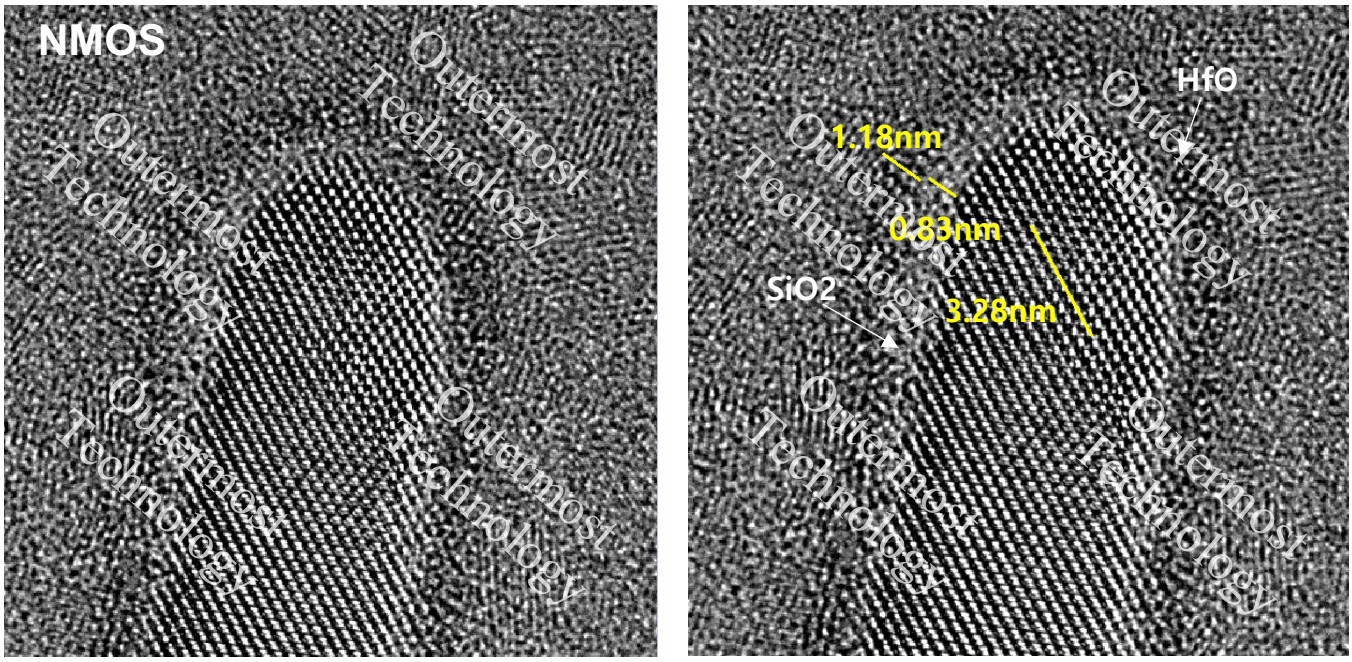

Figure 2.3.4 NMOS Si fin, HR-TEM cross-sectional image

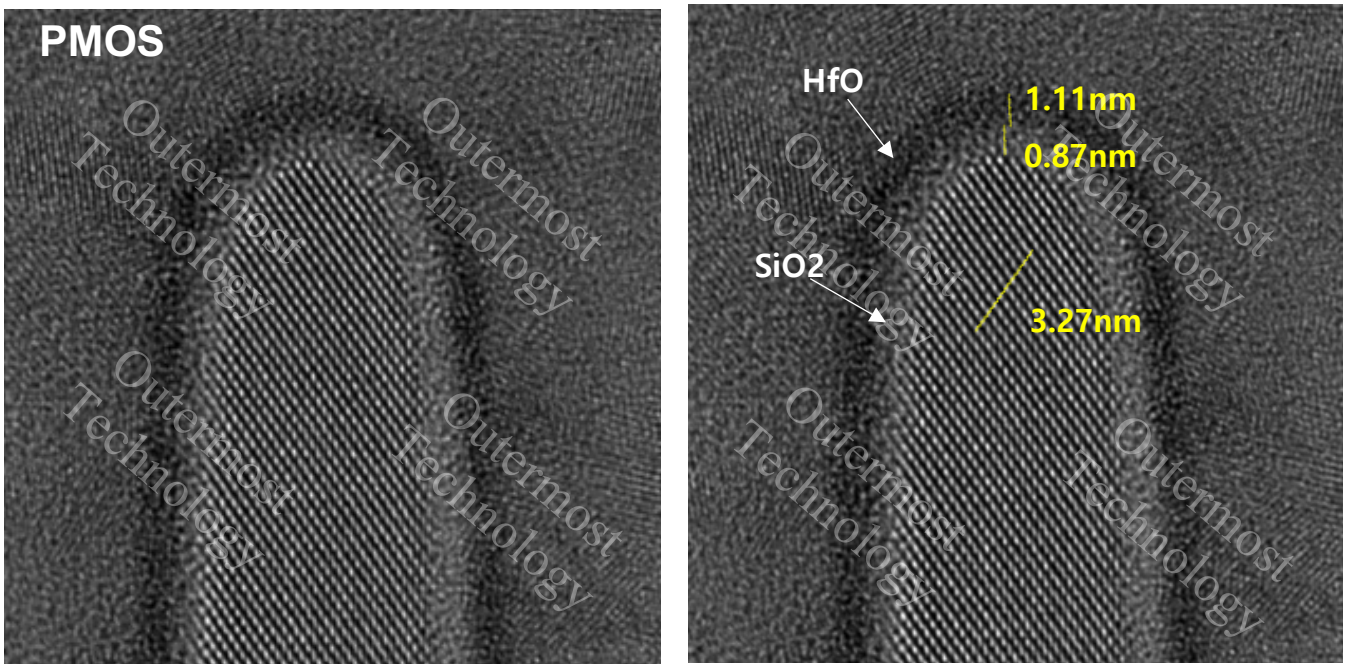

Figure 2.3.5 PMOS Si fin, HR-TEM cross-sectional image

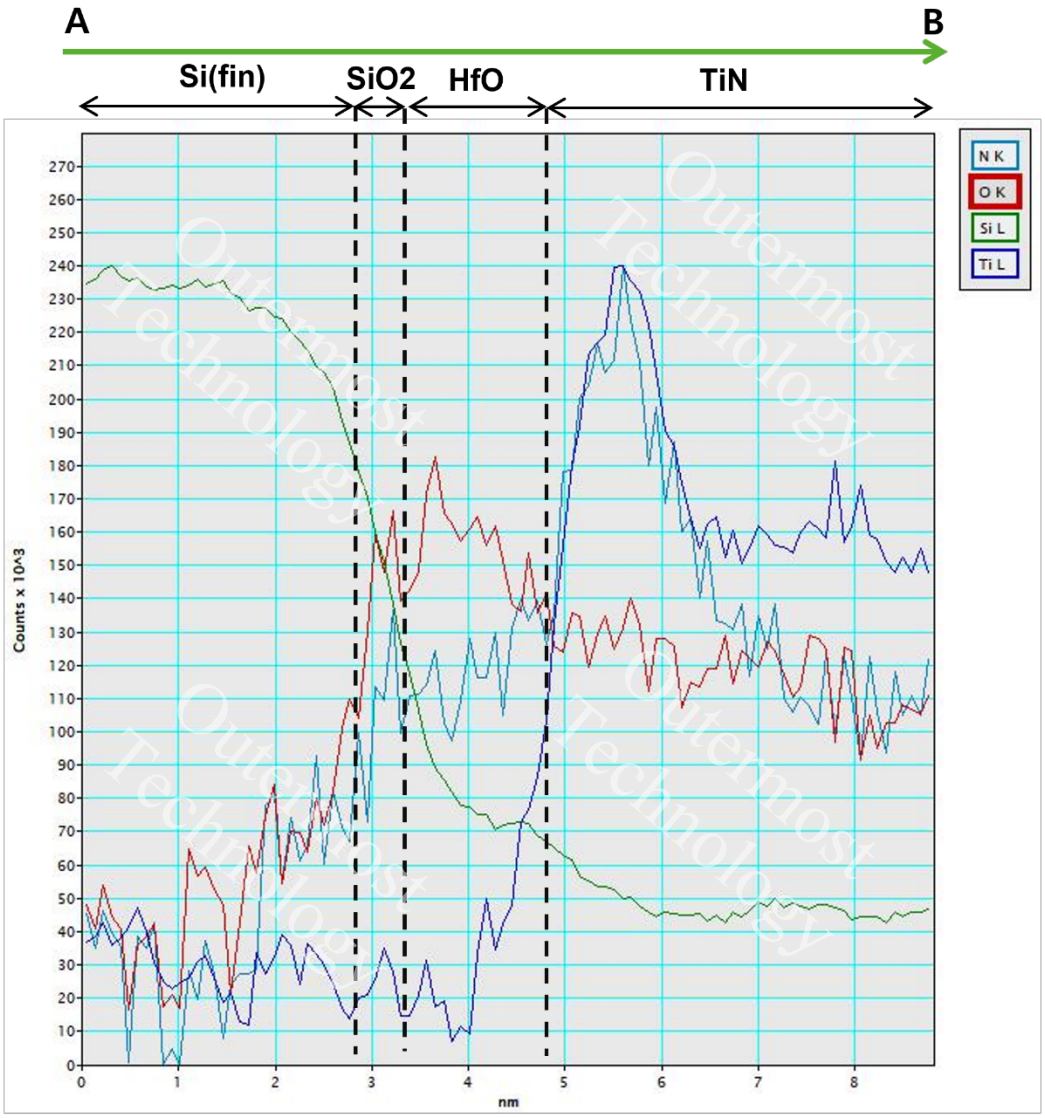

Figure 2.3.6 TEM-EELS profile from NMOS Fin

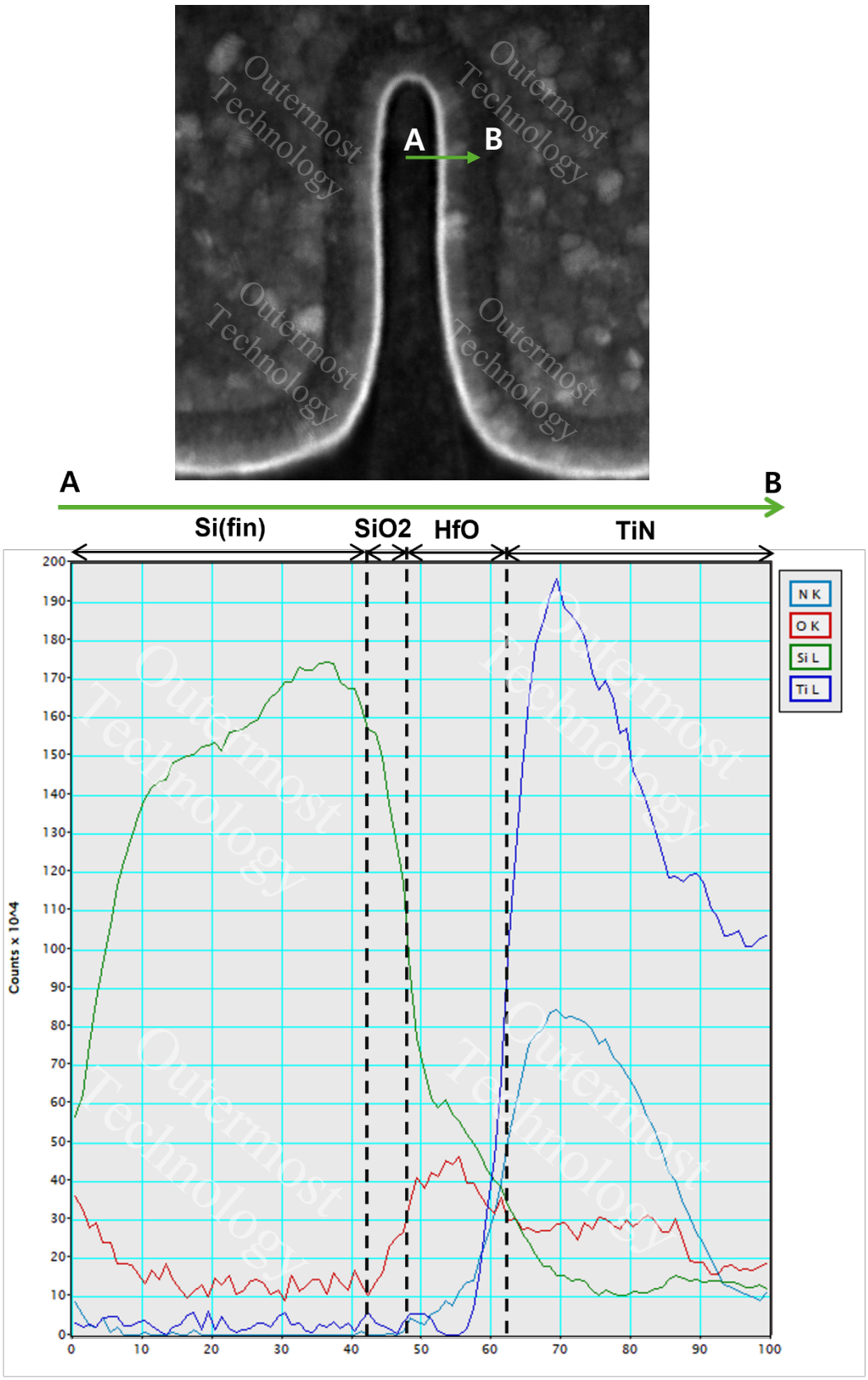

Figure 2.3.7 TEM-EELS profile from PMOS Fin

2.4 FinFET Transistor Process

FinFET Transistor Process Summary

Features	Details	NMOS	PMOS
FinFET Features	High K Oxide HfO_2	1.2 nm HfO_2 + 0.9 nm HfO_2	1.2 nm HfO_2 + 0.9 nm SiO_2
	Work Function	4 nm TiAlC	4 nm TiN
	Barrier Layer	6 nm Tin	6 nm TiN
	W Fill	W Fill	W Fill (not visible)
FinFET Size	Gate Pitch	78 nm	78 nm
	Gate Length	33 nm	30 nm
	Fin Pitch	49 nm	45nm
	Fin Width	8 nm	8 nm
	Fin Height	38 nm	37 nm

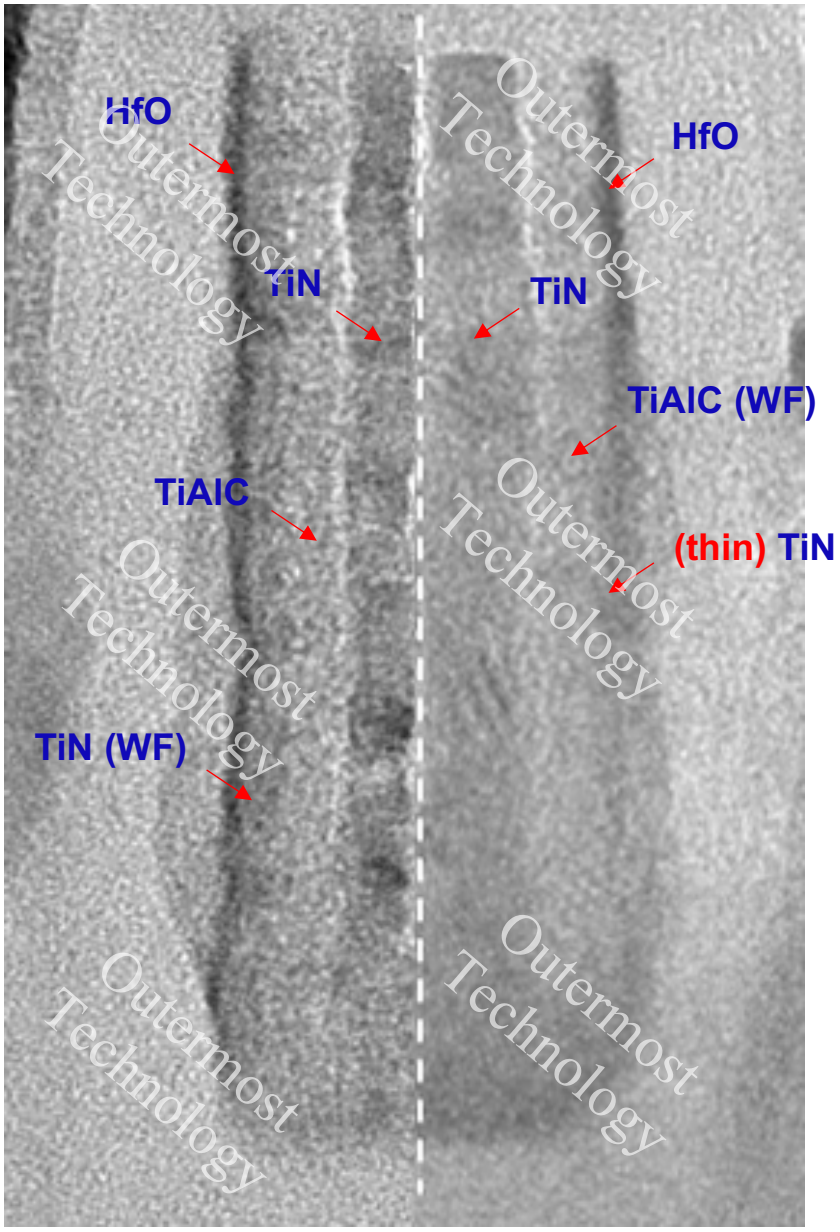

Figure 2.4.1 Metal gate comparison of PMOS and NMOS transistors, C ombined TEM cross sectional image

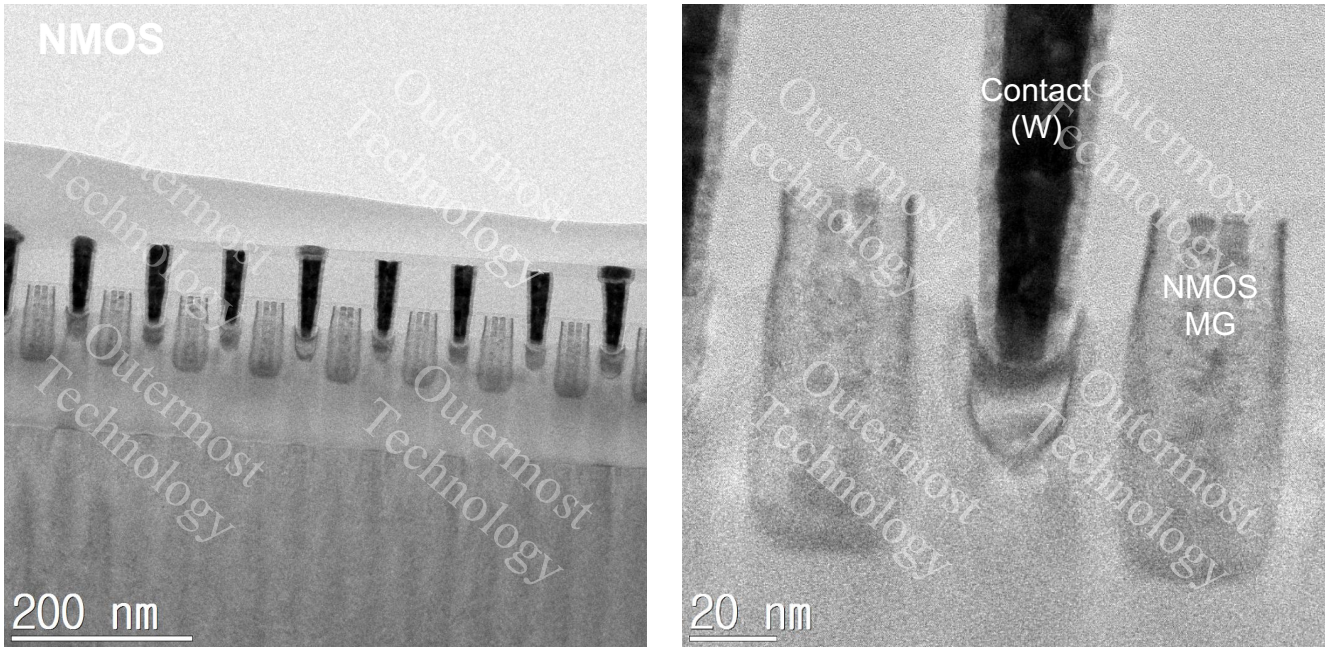

Figure 2.4.2 Overview of NMOS finFETs along fin direction, TEM cross-sectional image

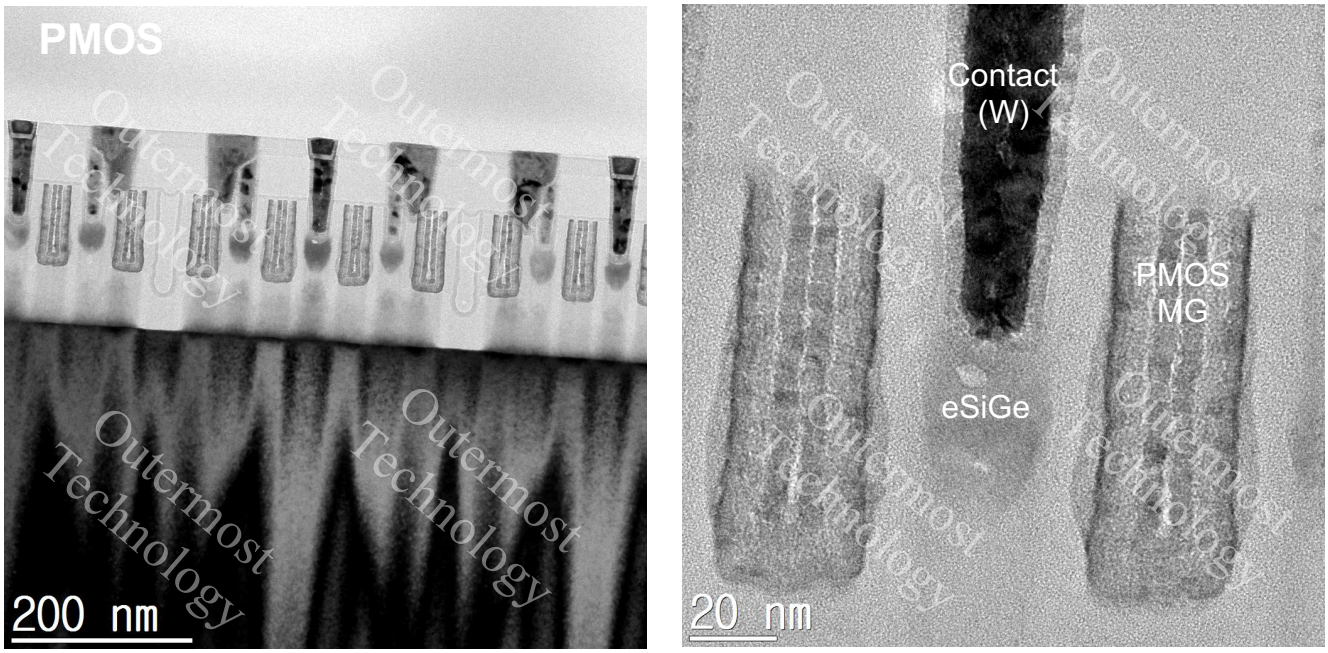

Figure 2.4.3 Overview of PMOS finFETs along fin direction, TEM cross-sectional image

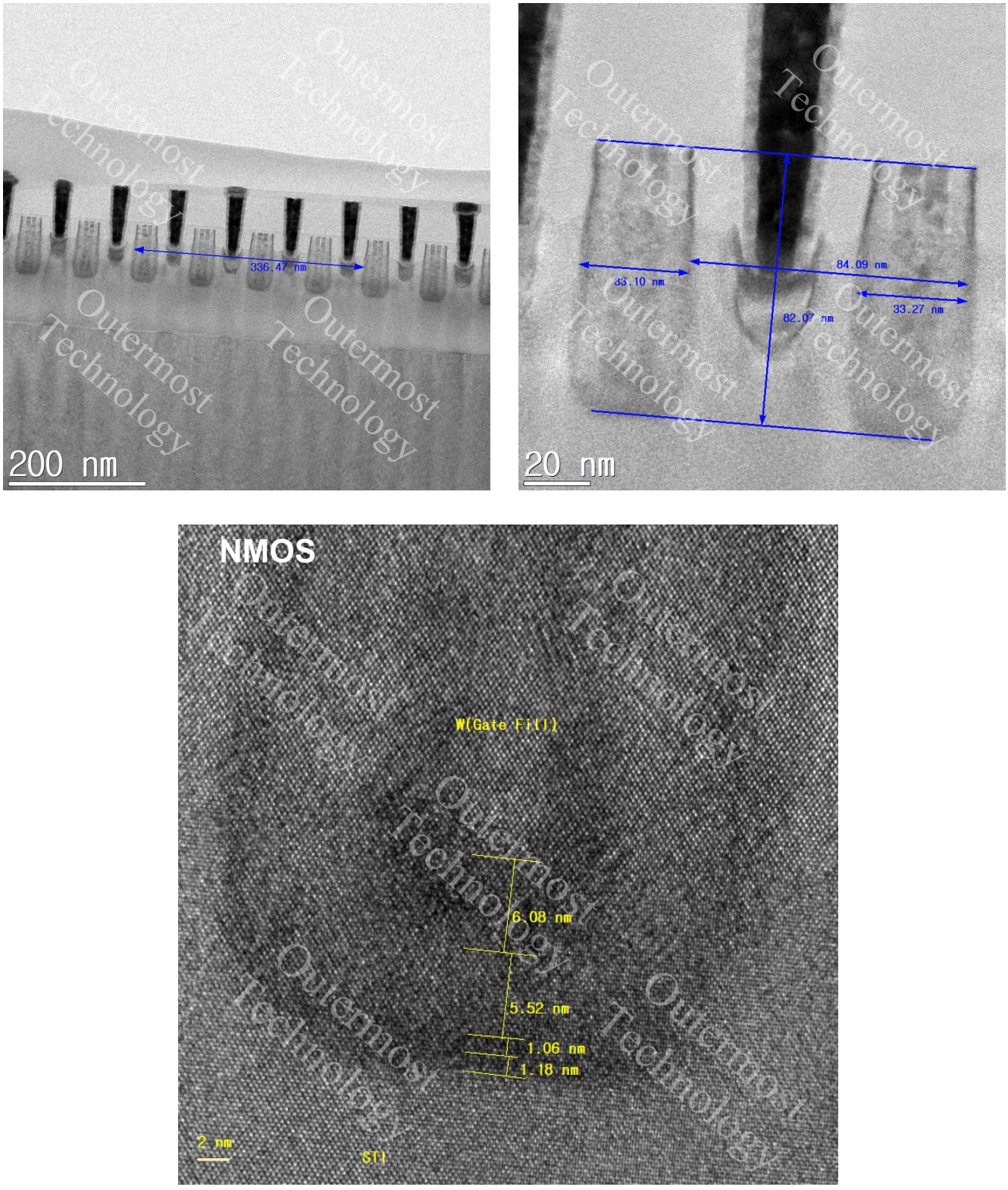

Figure 2.4.4 Overview of NMOS finFETs along fin direction, TEM cross-sectional image

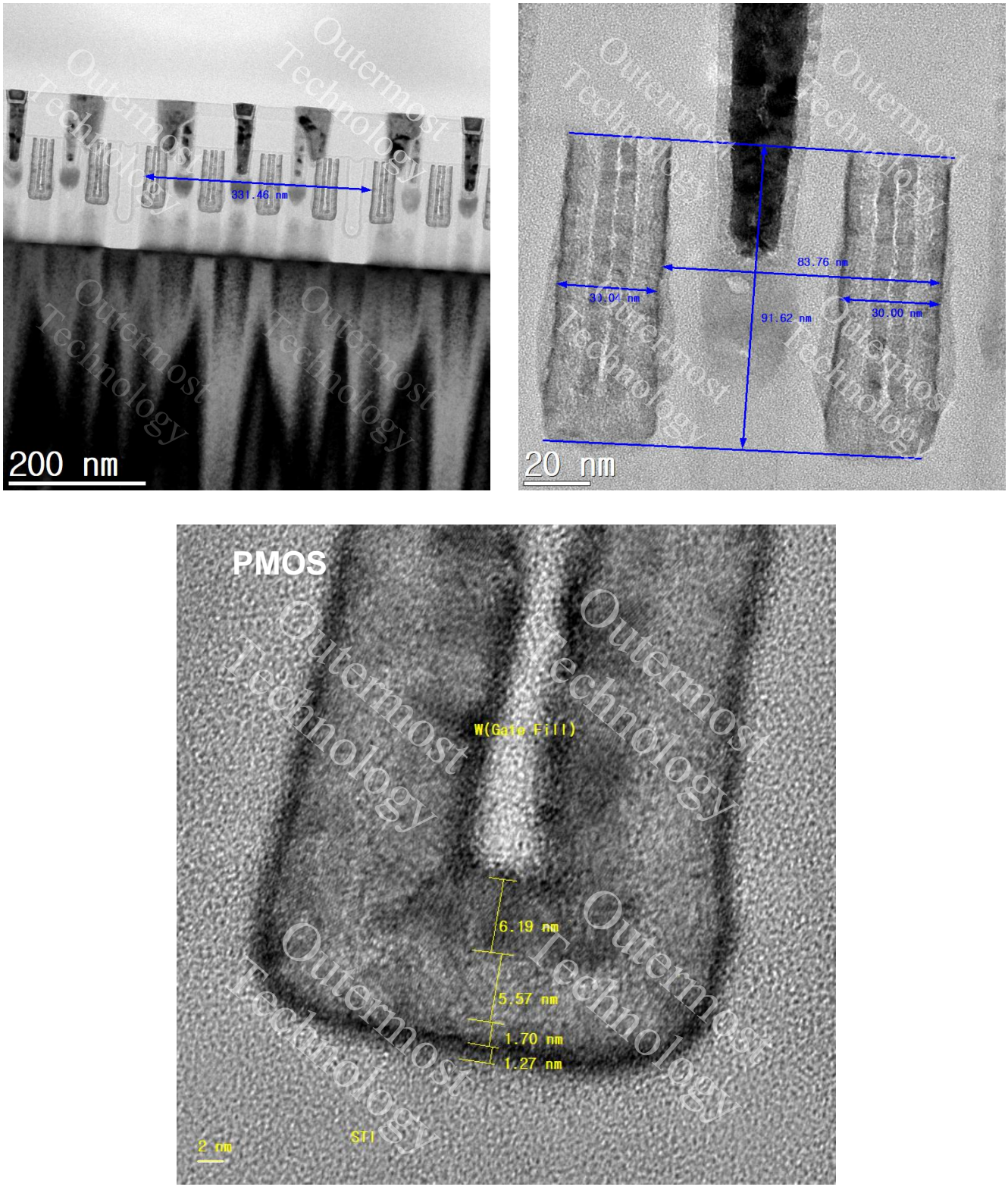

Figure 2.4.5 Overview of PMOS finFETs along fin direction, TEM cross-sectional image

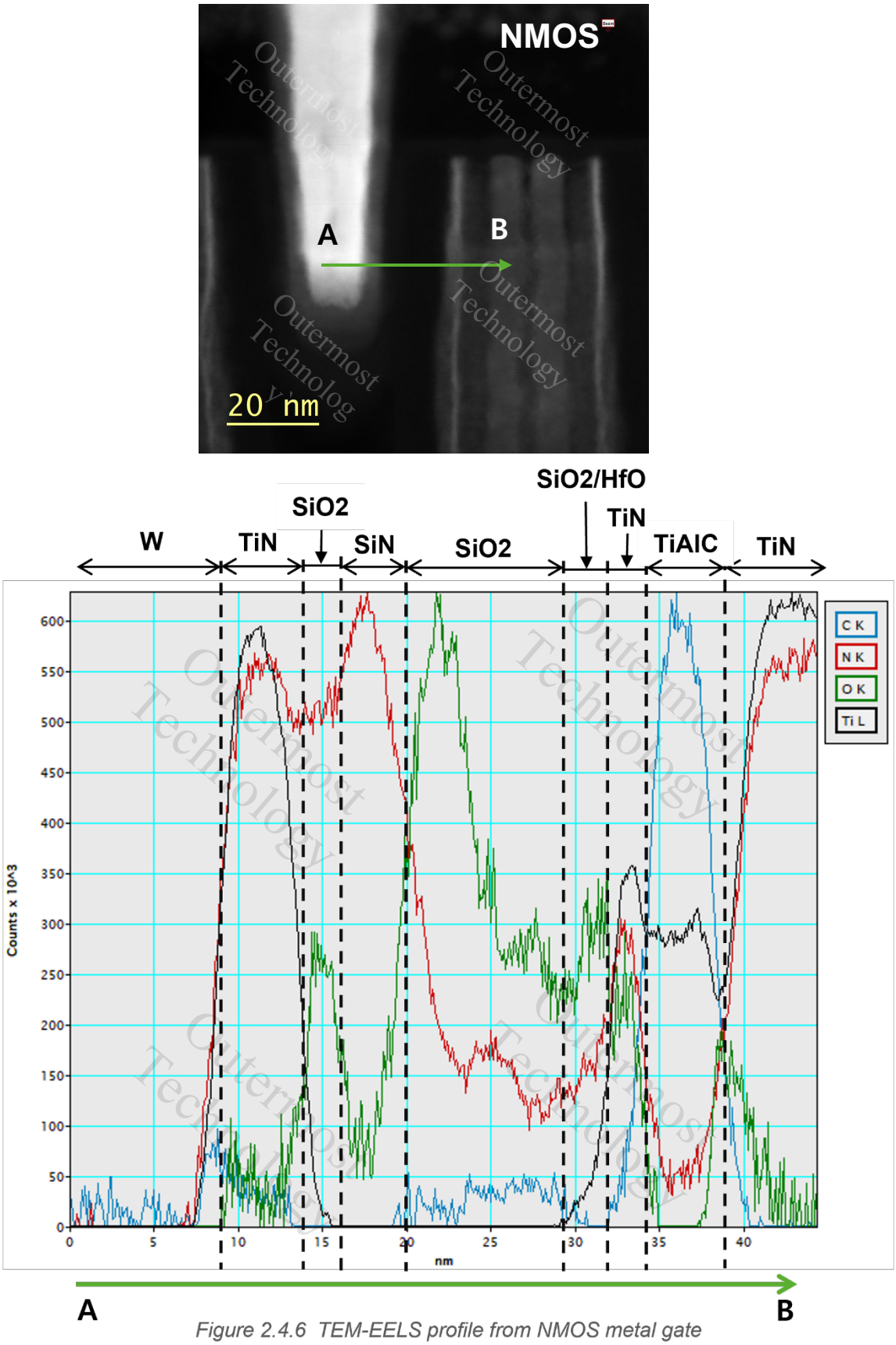

Figure 2.4.6 TEM-EELS profile from NMOS metal gate

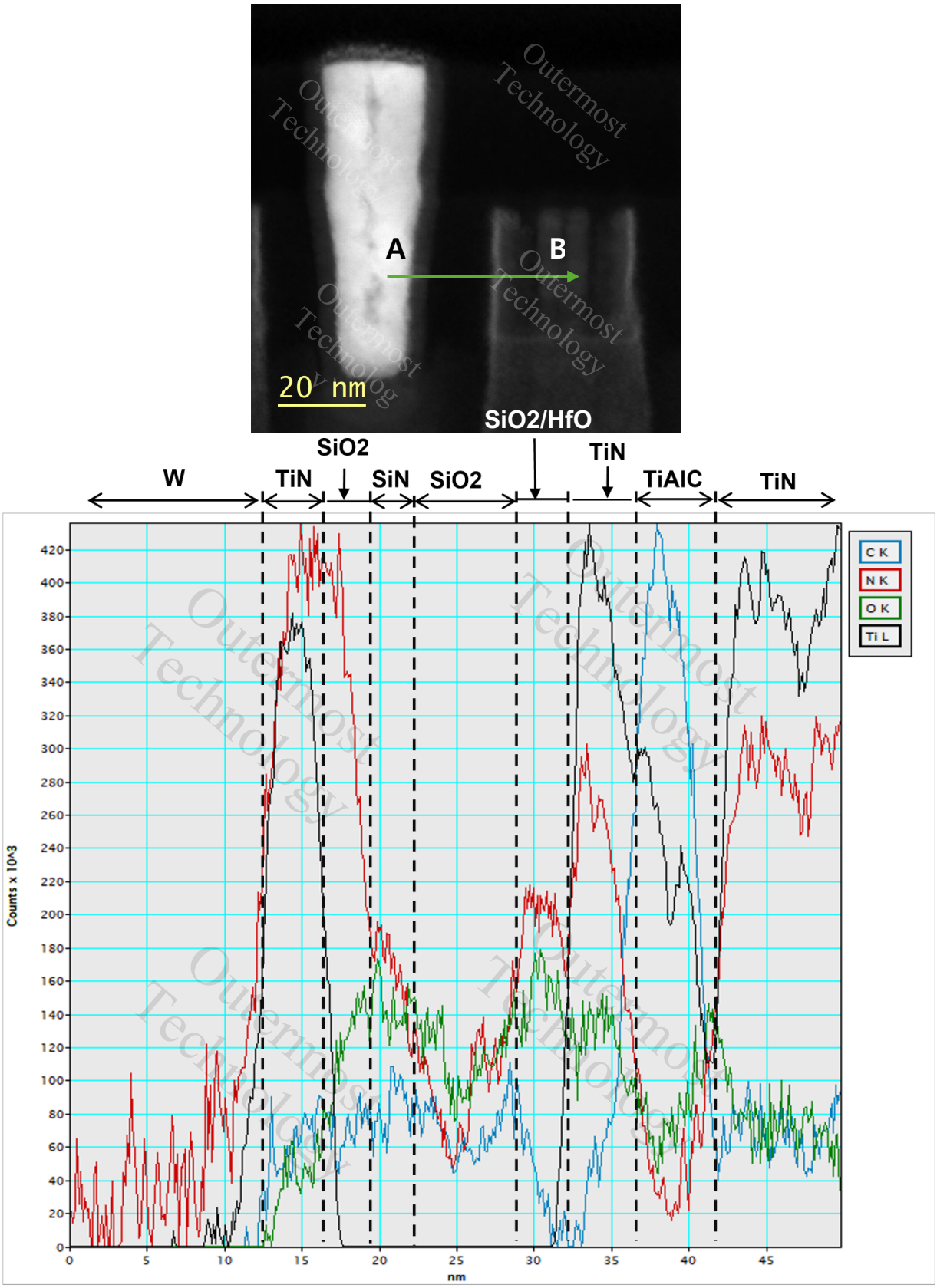

Figure 2.4.7 TEM-EELS profile from PMOS metal gate

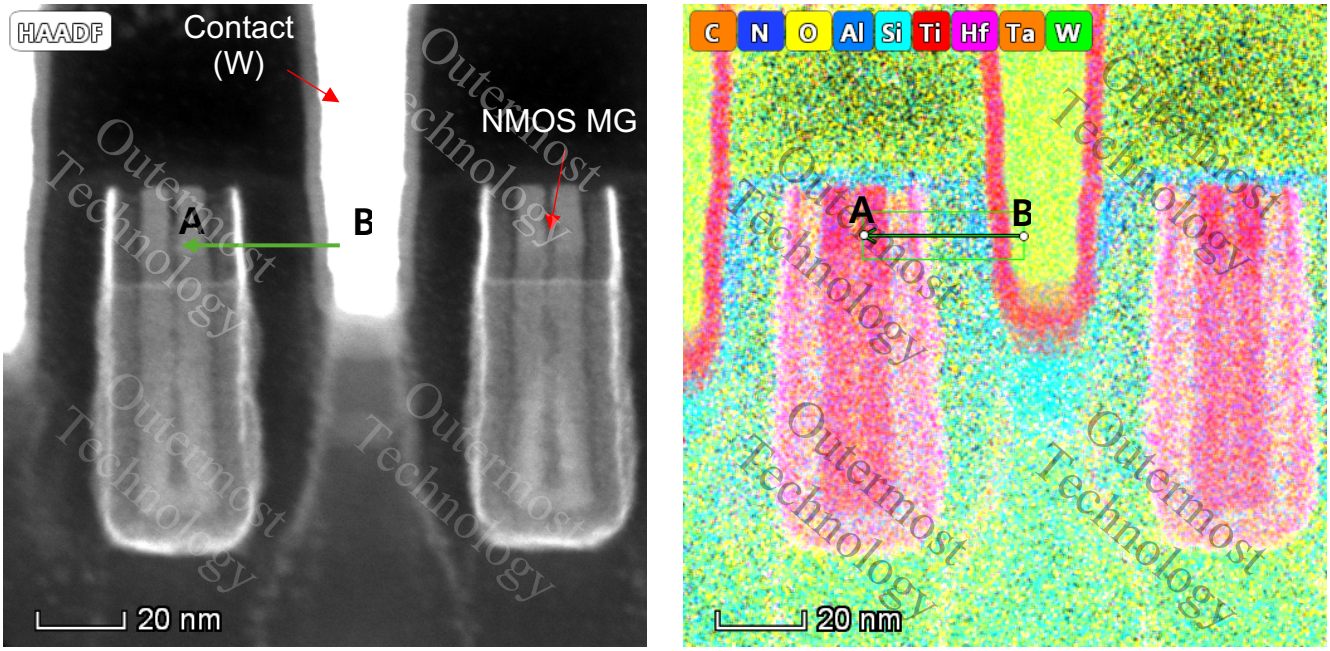

Figure 2.4.8 NMOS metal gate annotated with the EDS profile acquisition line, H AADF TEM cross section

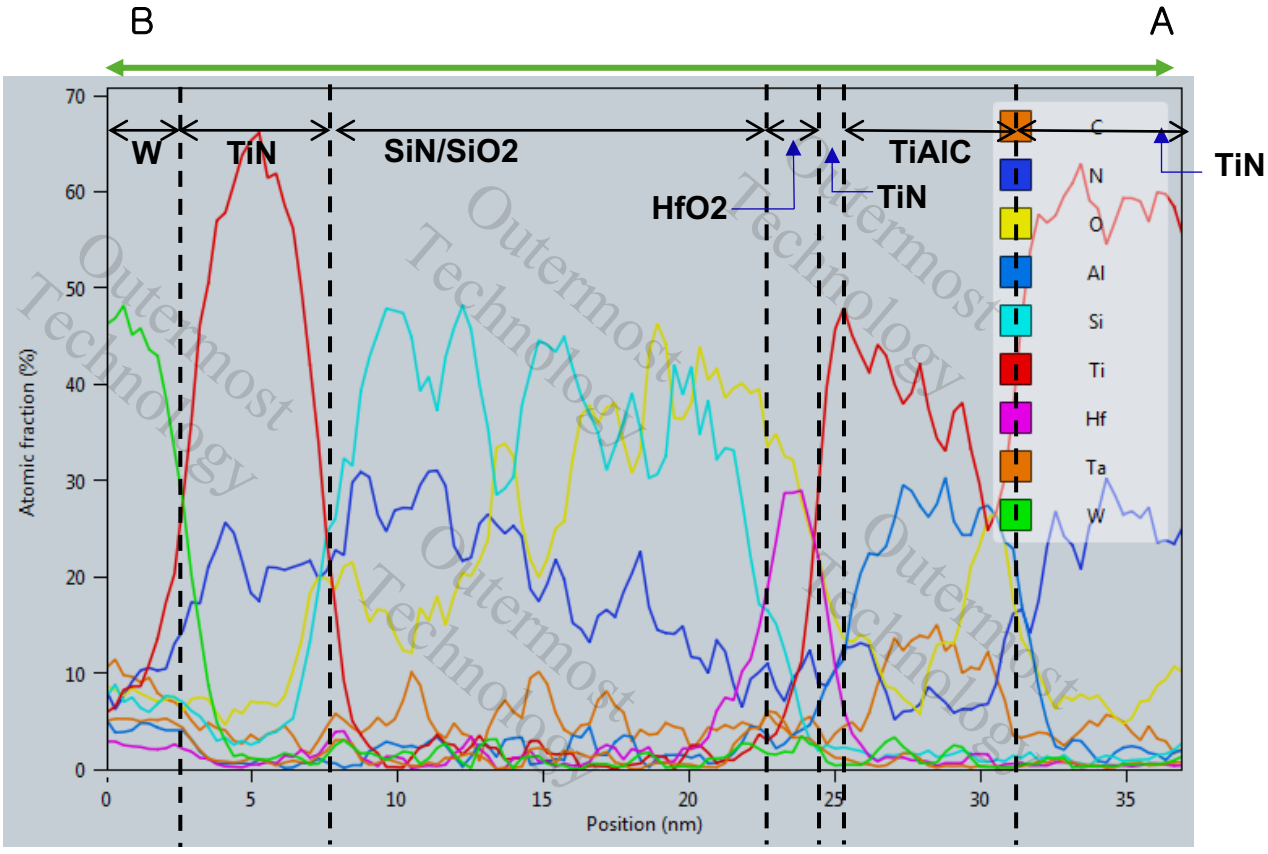

Figure 2.4.9 TEM-EDS profile from NMOS metal gate shown in Figure 2.5.6

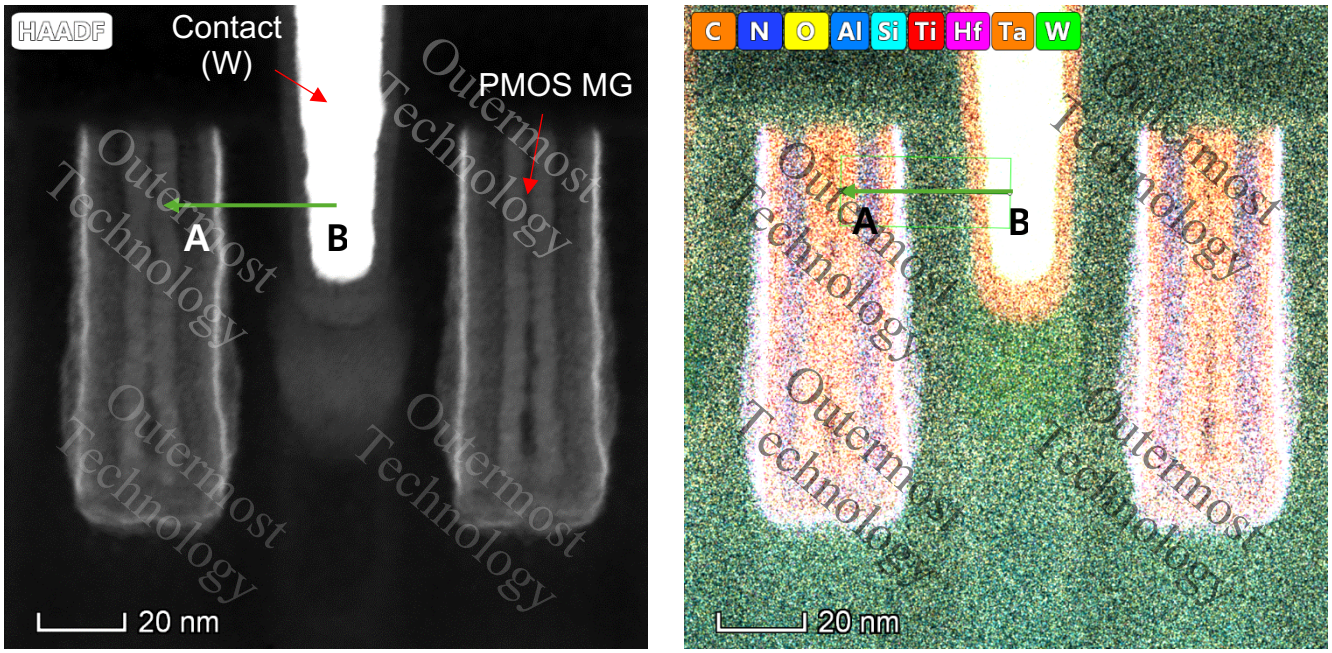

Figure 2.4.10 PMOS metal gate annotated with the EDS profile acquisition line, HAADF TEM cross section

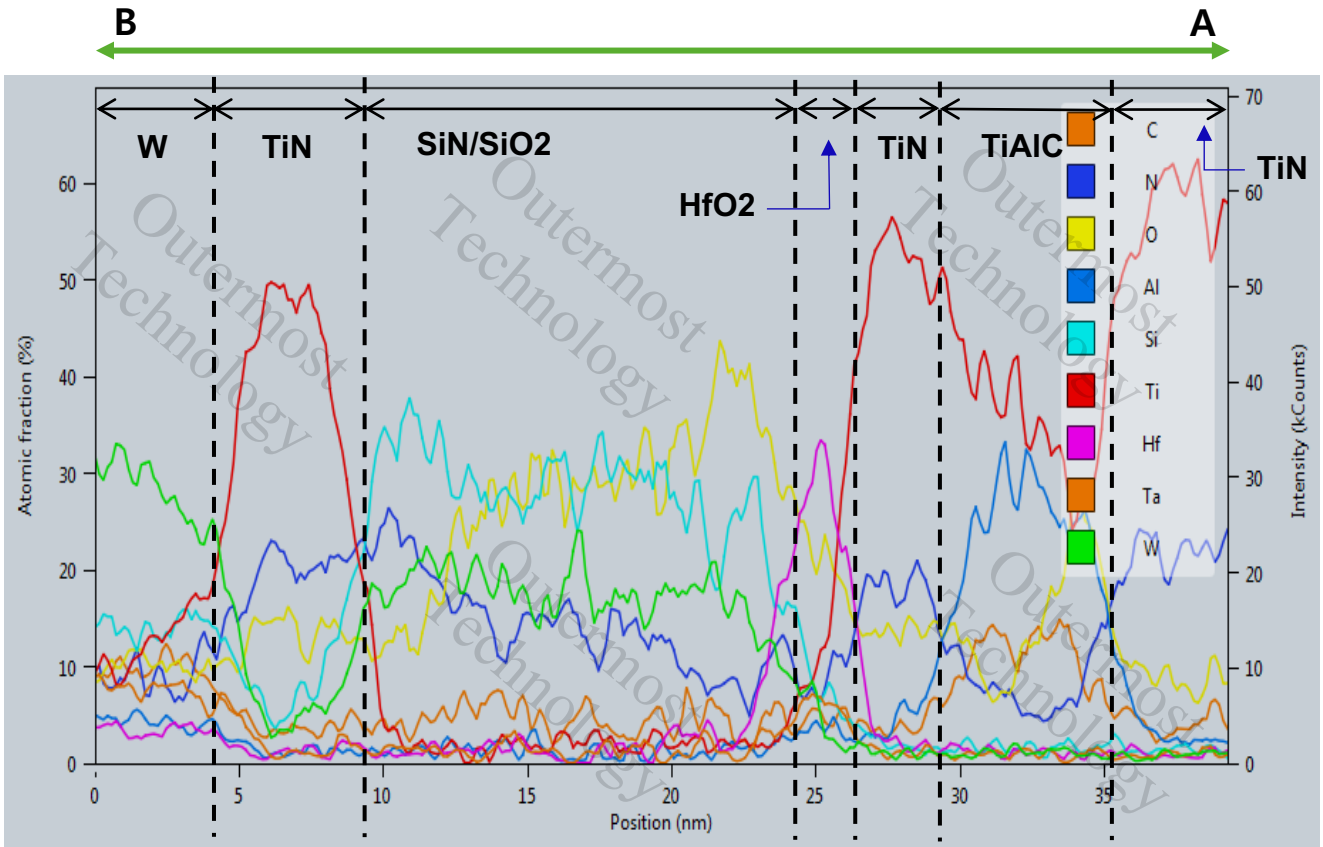

Figure 2.4.11 TEM-EDS profile from PMOS metal gate shown in Figure 2.5.8

2.5 Materials of Transistor

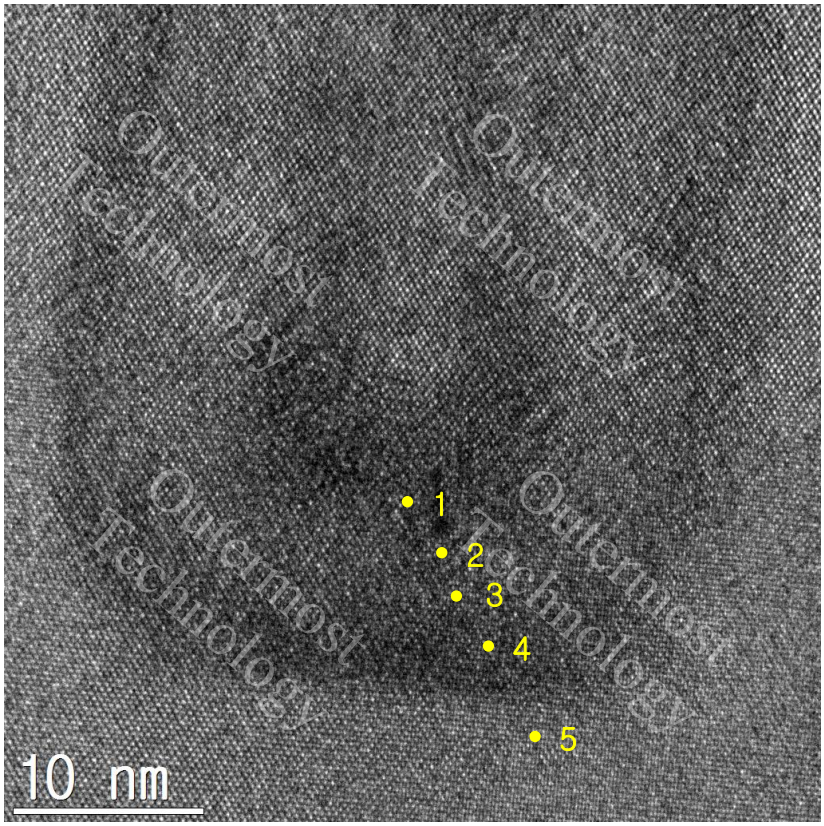

Figure 2.5.1 NMOS metal gate with TEM-EDS acquisition sites annotated

No.	Elements Detected	Layers & Likely composition
1	Ti, O, Si	-
2	Ti, O, Si, Al	TiN, TiAlC
3	Ti, O, Si, Al	TiAlC NMOS WF layer
4	Ti, O, Si	TiN
5	O, Si	SiO2

Figure 2.5.2 Summary of EDS Analysis from the locations indicated in Figure 2.5.1

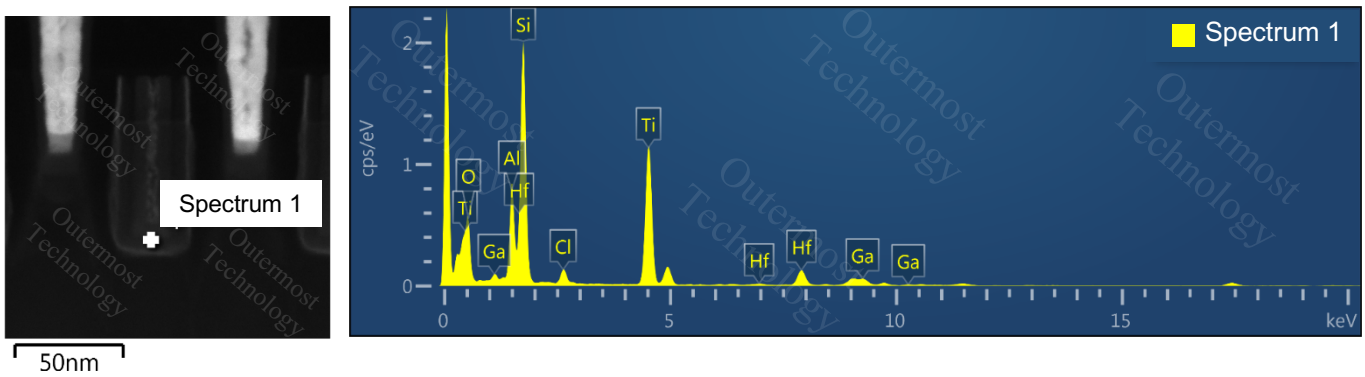

Figure 2.5.3 EDS spectrum from location 1 in Figure 2.6.1

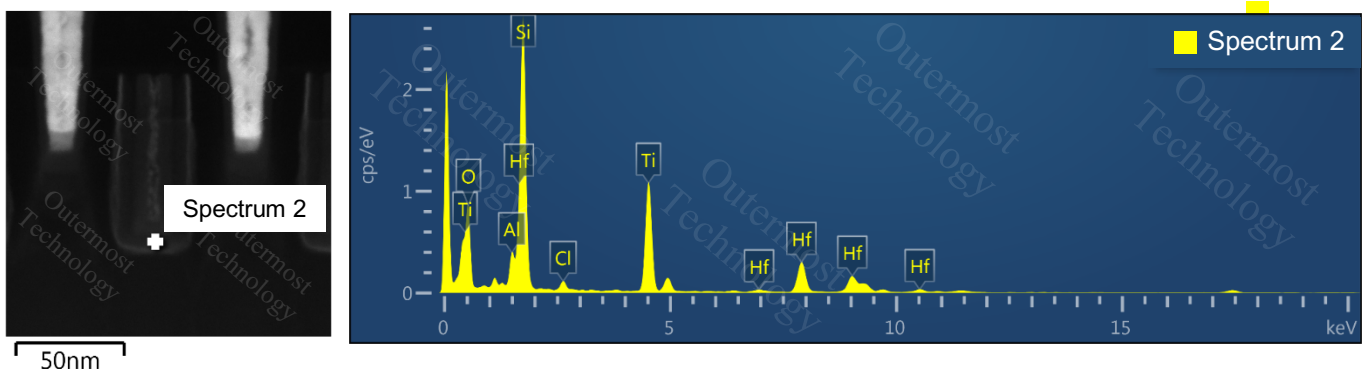

Figure 2.5.4 EDS spectrum from location 2 in Figure 2.6.1

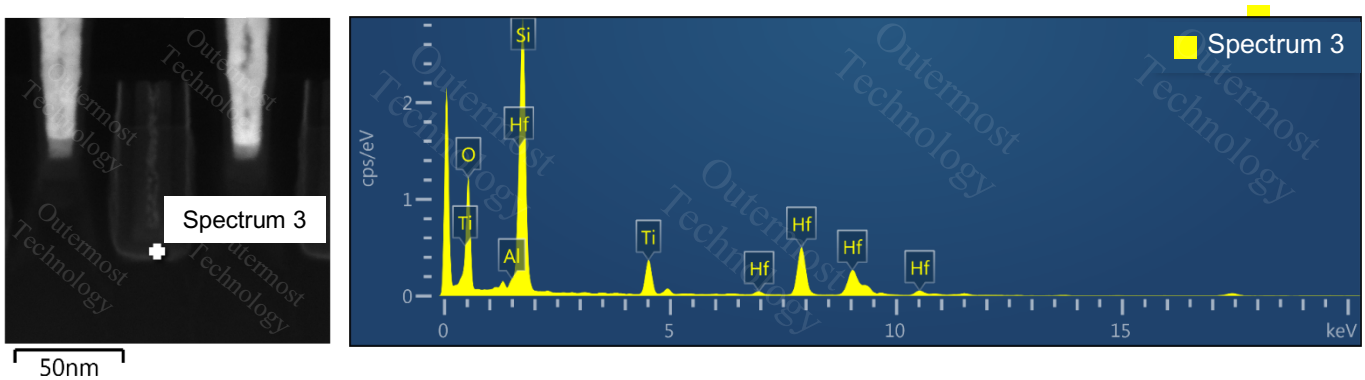

Figure 2.5.5 EDS spectrum from location 3 in Figure 2.6.1

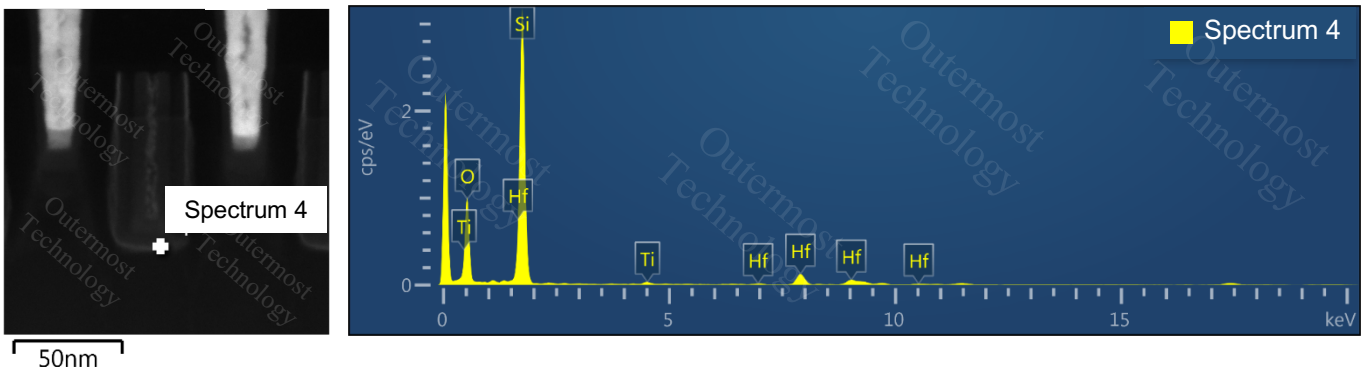

Figure 2.5.6 EDS spectrum from location 4 in Figure 2.6.1

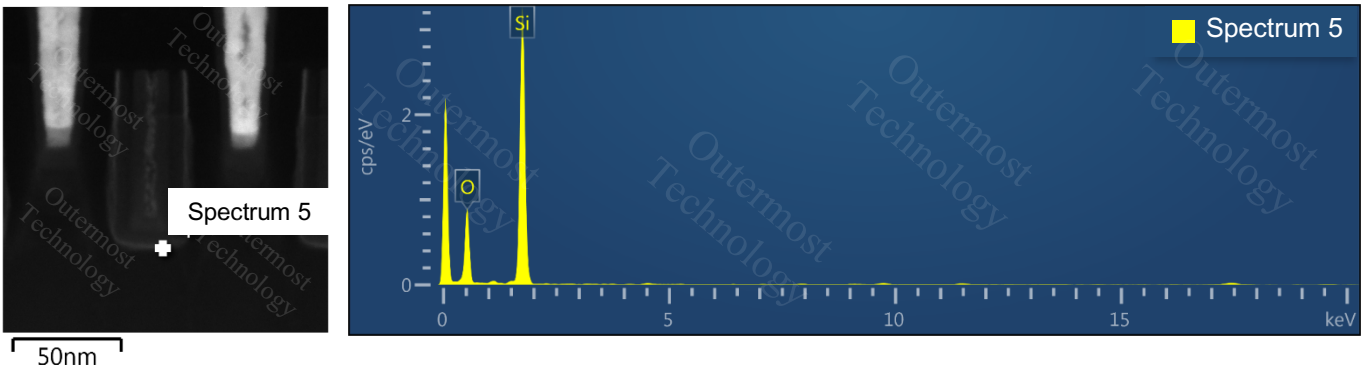

Figure 2.5.7 EDS spectrum from location 5 in Figure 2.6.1

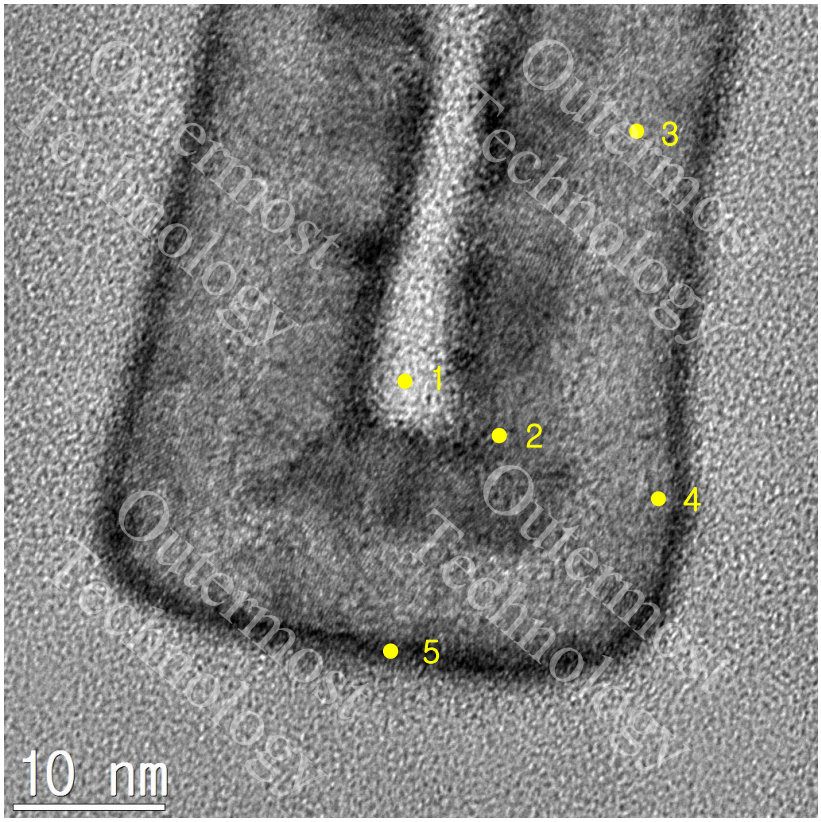

Figure 2.5.8 PMOS metal gate with TEM-EDS acquisition sites annotated

No.	Elements Detected	Layers & Likely composition
1	Si, O, W	W gate fill
2	Ti, N, W	TiN
3	Ti, C, Si, Al	TiAlC
4	Ti, N, O, Si	TiN
5	Hf, O, Ti, Si	HfO2

Figure 2.5.9 Summary of EDS Analysis from the locations indicated in Figure 2.6.8

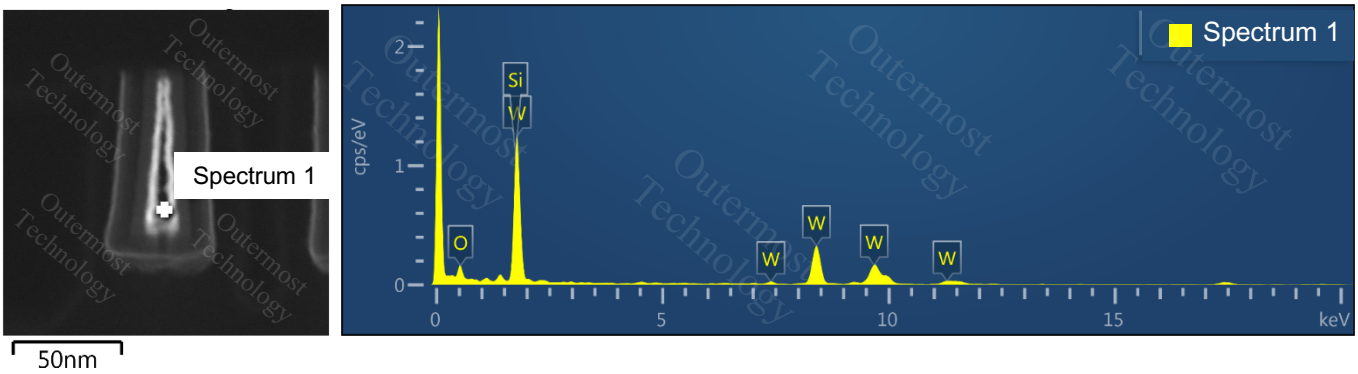

Figure 2.5.10 EDS spectrum from location 1 in Figure 2.6.8

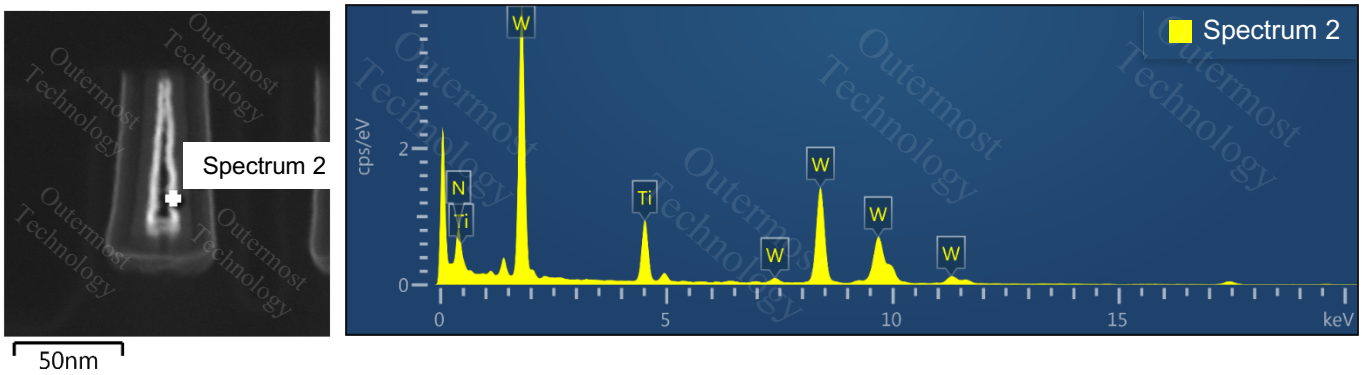

Figure 2.5.11 EDS spectrum from location 2 in Figure 2.6.8

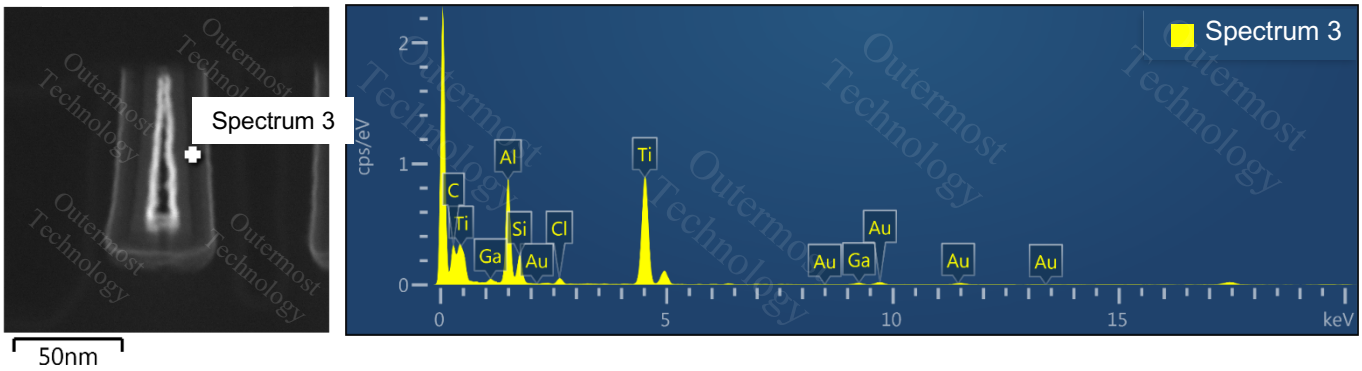

Figure 2.5.12 EDS spectrum from location 3 in Figure 2.6.8

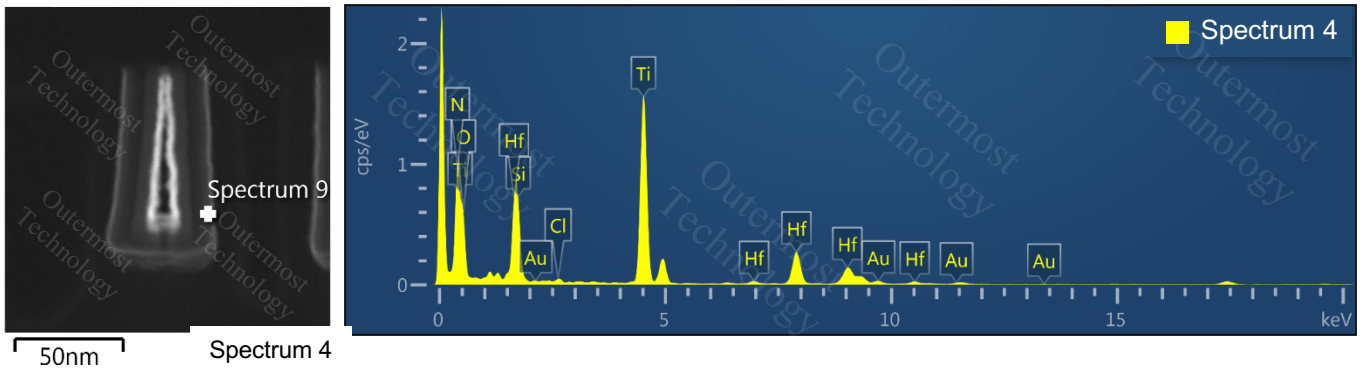

Figure 2.5.13 EDS spectrum from location 4 in Figure 2.6.8

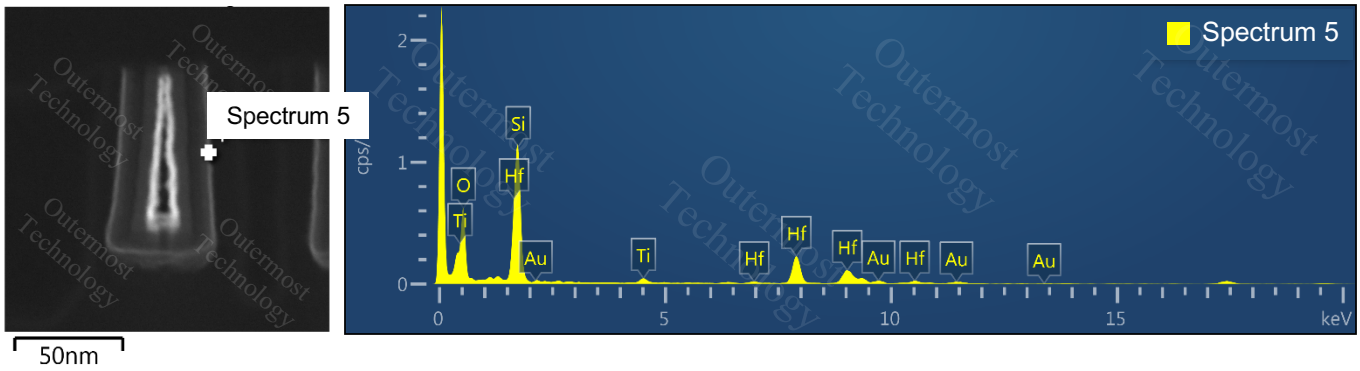

Figure 2.5.14 EDS spectrum from location 5 in Figure 2.6.8

3.0 Functional & Memory Block Analysis

3.1 Functional Block Area

Functional Area	Area(mm²)	% of Total Area
Die Size	18.20	100
Memory Block	3.11	17.1
Logic Block	9.76	53.6
IP Block	3.35	18.4
I/O Block	1.61	8.8
Others	0.36	2.0

Figure 3.1.1: Function block areas

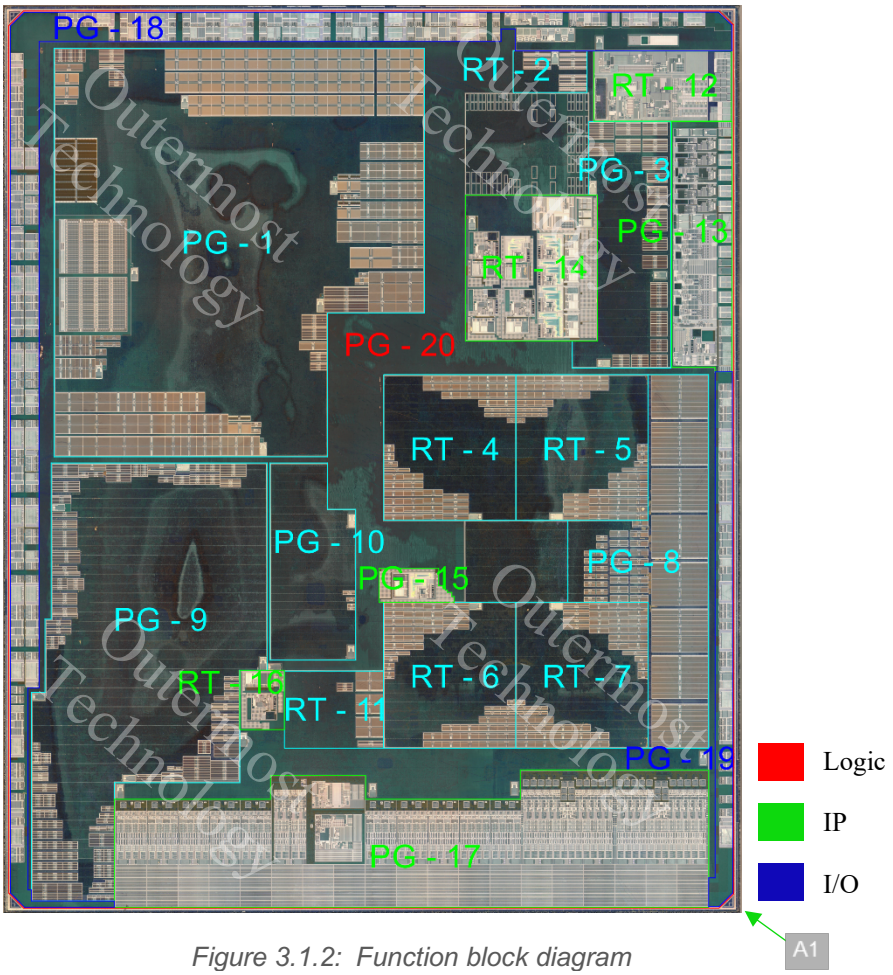

Figure 3.1.2: Function block diagram

4.0 SRAM Cell Layout Analysis

4.1 Memory Block Area

Memory Area	Cell Size (μm^2)	# of Total Bit (Kbit)	Total Area per Memory Type (mm^2)	% of Total Die Area
6T_A SRAM	0.0842	10,310	1.85	10.2
6T_B SRAM	0.0642	4,551	0.53	2.9
8T SRAM	0.1450	1,537	0.61	3.4

Figure 4.1.1: Memory block areas

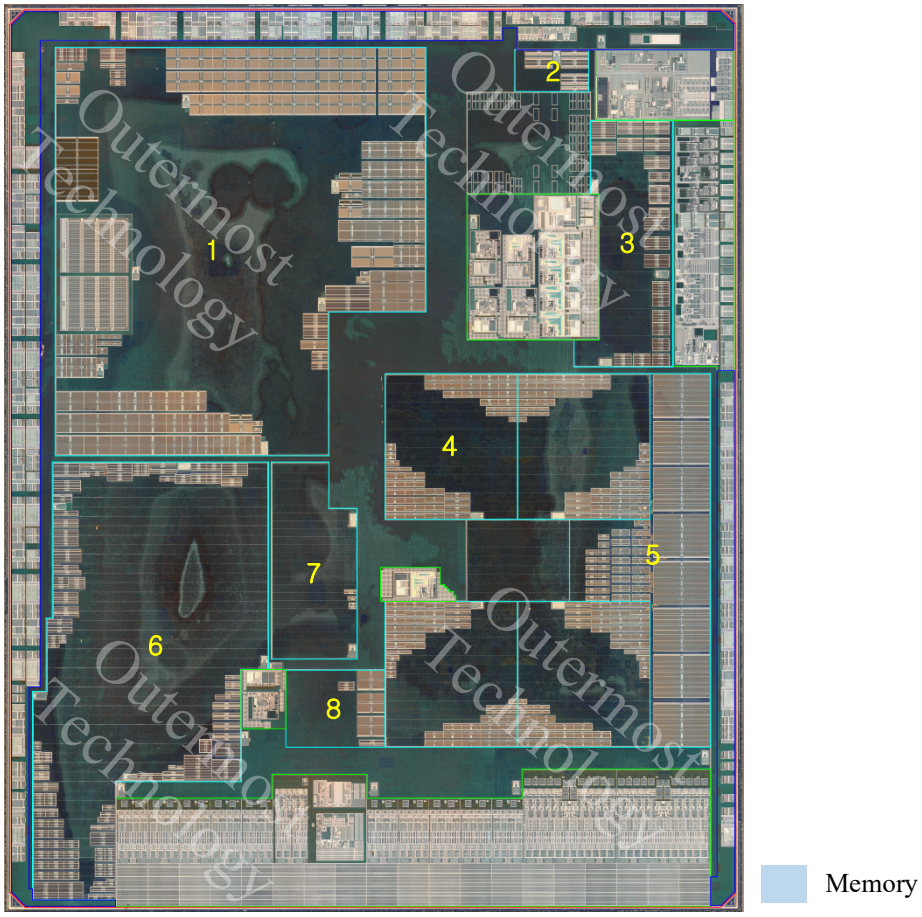

Figure 4.1.2: Memory block diagram

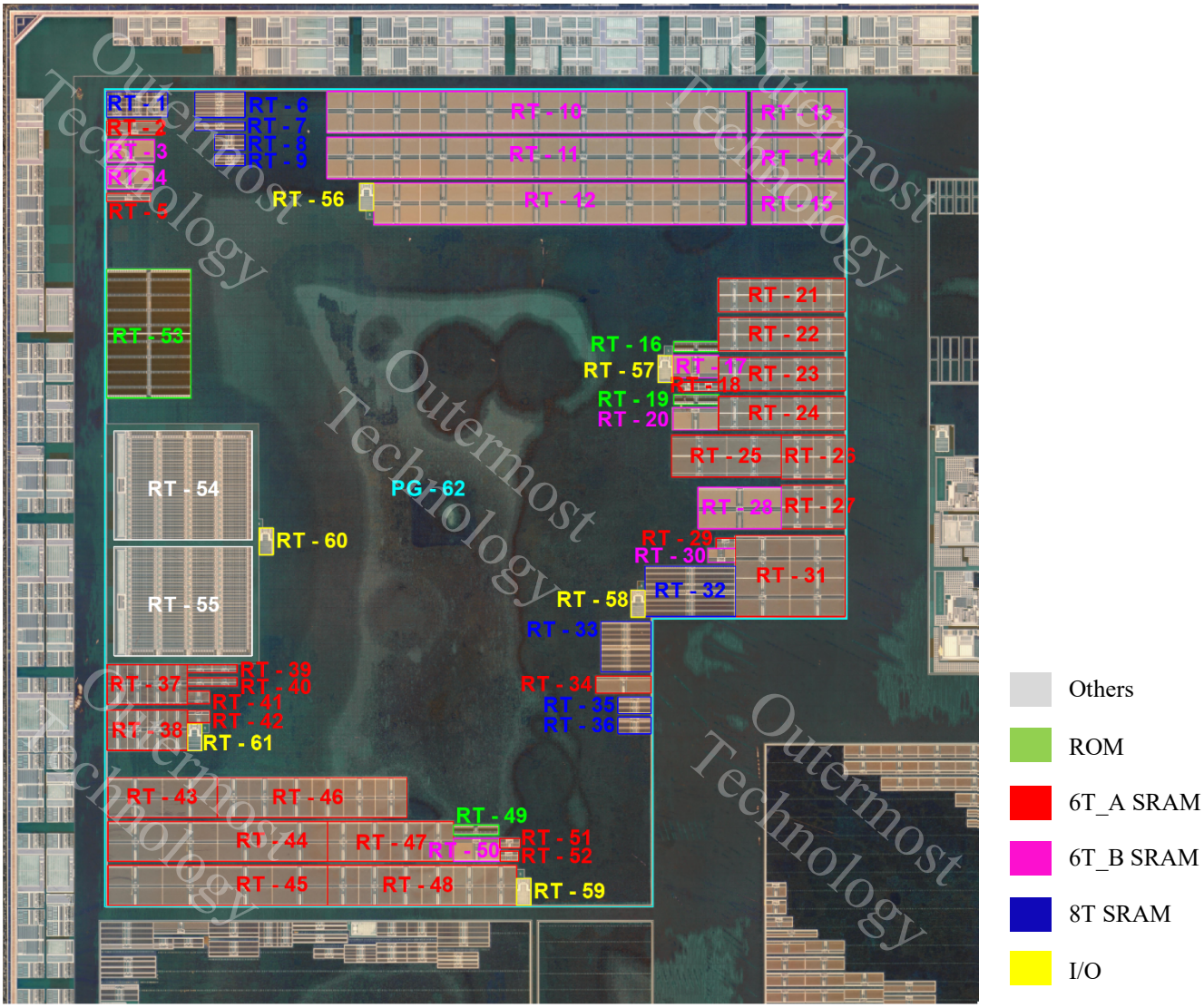

Figure 4.1.3: Block #1

Block No.	No.	No. Memory Type	Physical Size	Cell Size			
			X * Y (um2)	X(bit)	Y(bit)	Block (ea)	Total(bit)
Block #1	RT1	8T	10512.96	62	16	12	11,904
	RT2	6T_A	5518.96	128	128	2	32,768
	RT3	6T_B	7596.06	132	266	2	70,224
	RT4	6T_B	7287.61	132	266	2	70,224
	RT5	6T_A	2559.89	96	32	2	6,144
	RT6	8T	8949.6	64	16	4	4,096
	RT7	8T	2931.76	64	32	2	4,096
	RT8	8T	3359.17	32	64	4	8,192
	RT9	8T	2457.17	32	32	4	4,096
	RT10	6T_B	120268.63	130	254	36	1,188,720
	RT11	6T_B	120268.63	130	254	36	1,188,720
	RT12	6T_B	106759.12	130	254	32	1,056,640
	RT13	6T_B	26849.09	130	254	8	264,160
	RT14	6T_B	26849.09	130	254	8	264,160
	RT15	6T_B	26849.09	130	254	8	264,160
	RT17	6T_B	7056.38	130	258	2	67,080
	RT18	6T_A	2530.45	34	48	4	6,528
	RT20	6T_B	7056.38	130	258	2	67,080
	RT21	6T_A	29317.64	66	188	16	198,528
	RT22	6T_A	29317.64	66	188	16	198,528
	RT23	6T_A	29317.64	66	188	16	198,528
	RT24	6T_A	29317.64	66	188	16	198,528
	RT25	6T_A	31902.87	130	250	8	260,000
	RT26	6T_A	19311.44	66	250	8	132,000
	RT27	6T_A	19311.44	66	250	8	132,000
	RT28	6T_A	24003.2	208	250	4	208,000
	RT29	6T_B	1391.31	40	66	2	5,280
	RT30	6T_A	2638.63	52	126	2	13,104
	RT31	6T_B	61385.43	164	260	2	85,280
	RT32	6T_A	31323.58	130	248	16	515,840
	RT33	8T	17539.3	128	62	16	126,976
	RT34	8T	6508.2	66	60	2	7,920
	RT35	6T_A	3721.79	130	188	4	97,760
	RT36	8T	3721.79	36	62	4	8,928
	RT37	8T	22326.65	36	62	16	35,712
	RT38	6T_A	22326.65	32	250	16	128,000
	RT39	6T_A	2803.86	32	250	2	16,000
	RT40	6T_A	2803.86	50	64	2	6,400
	RT41	6T_A	1911.72	50	64	2	6,400
	RT42	6T_A	1911.72	40	124	2	9,920
	RT43	6T_A	30120.56	40	124	8	39,680
	RT44	6T_A	60486.01	130	250	16	520,000
	RT45	6T_A	60486.01	130	250	16	520,000
	RT46	6T_A	52200.81	130	250	24	780,000
	RT47	6T_A	34732.52	66	250	24	396,000
	RT48	6T_A	52200.81	66	250	16	264,000
	RT50	6T_B	7336.77	132	260	2	68,640
	RT51	6T_A	1330.32	32	48	2	3,072
	RT52	6T_A	1299.97	28	64	2	3,584

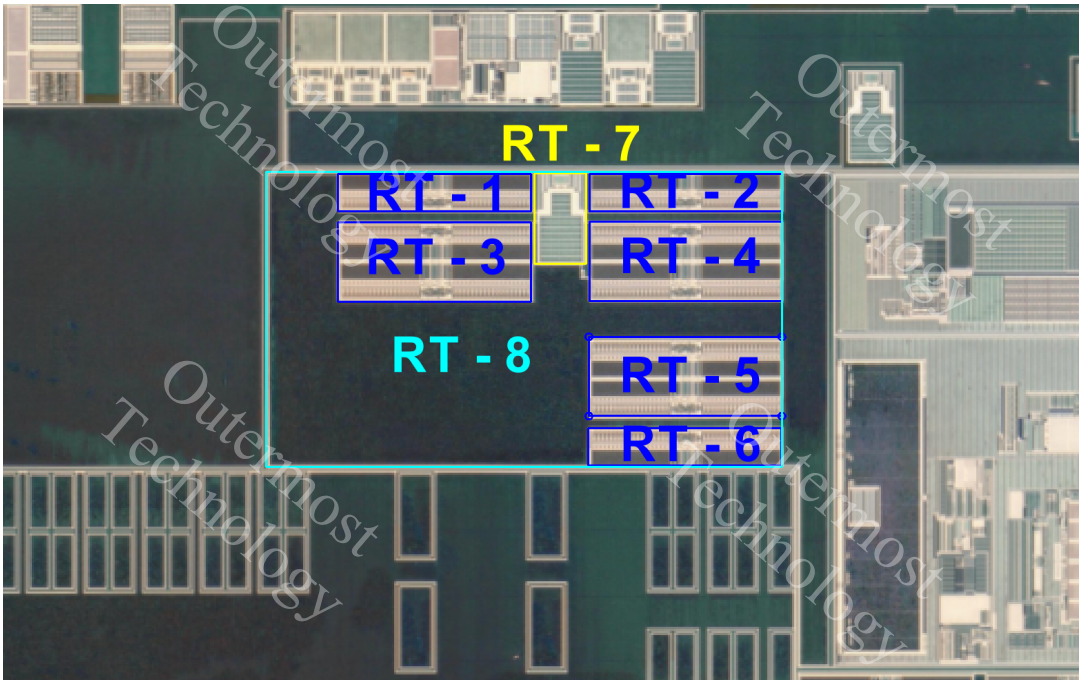

Figure 4.1.4: Block #2

Block No.	No.	No. Memory Type	Physical Size	Cell Size			
			X * Y (um2)	X(bit)	Y(bit)	Block (ea)	Total(bit)
Block #2	RT1	8T	4074.7	74	62	2	9,176
	RT2	8T	4074.7	74	62	2	9,176
	RT3	8T	8658.74	74	62	4	18,352
	RT4	8T	8658.74	74	62	4	18,352
	RT5	8T	8658.74	74	62	4	18,352
	RT6	8T	4074.7	74	62	2	9,176

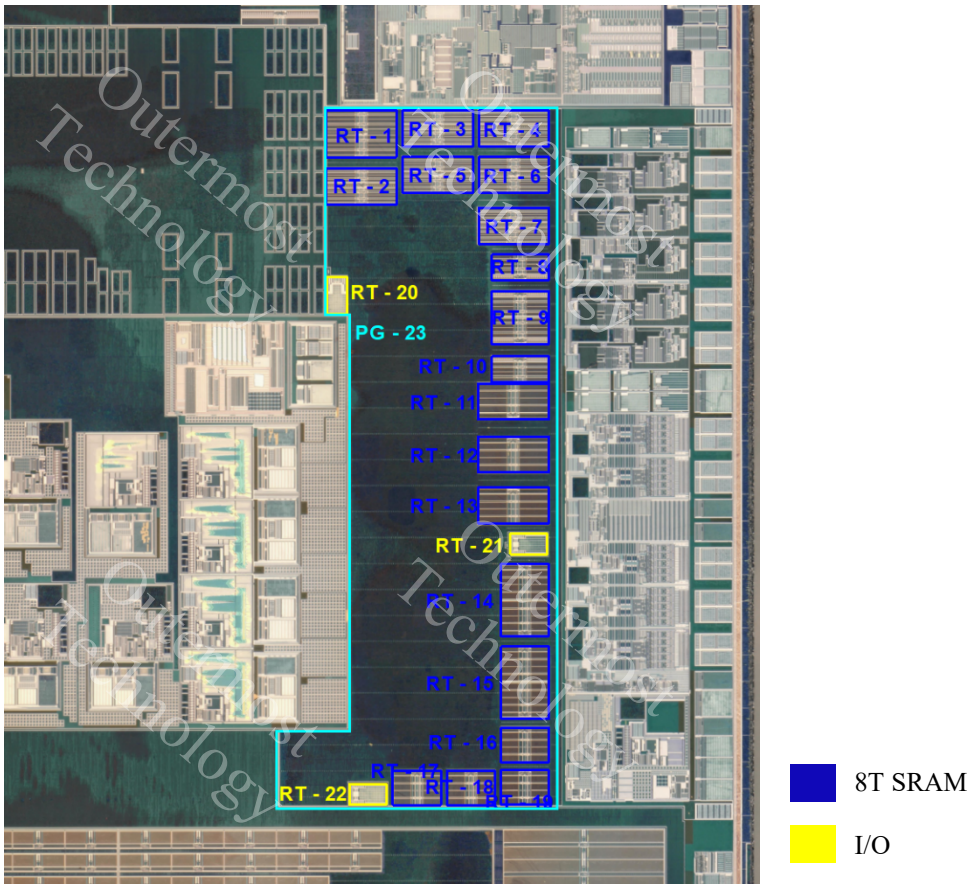

Figure 4.1.5: Block #3

Block No.	No.	No. Memory Type	Physical Size	Cell Size			
			X * Y (um2)	X(bit)	Y(bit)	Block (ea)	Total(bit)
Block #3	RT1	8T	11374.02	66	32	16	33,792
	RT2	8T	8733.62	66	16	16	16,896
	RT3	8T	8733.62	66	16	16	16,896
	RT4	8T	8733.62	66	16	16	16,896
	RT5	8T	8733.62	66	16	16	16,896
	RT6	8T	8733.62	66	16	16	16,896
	RT7	8T	8733.62	66	16	16	16,896
	RT8	8T	5062.33	66	16	16	16,896
	RT9	8T	10454.83	50	32	8	12,800
	RT10	8T	5062.33	50	32	8	12,800
	RT11	8T	8769.53	66	62	8	32,736
	RT12	8T	8769.53	66	62	8	32,736
	RT13	8T	8769.53	66	62	8	32,736
	RT14	8T	11900.02	40	62	16	39,680
	RT15	8T	11900.02	40	62	16	39,680
	RT16	8T	5706.43	40	62	8	19,840
	RT17	8T	5706.43	40	62	8	19,840
	RT18	8T	5706.43	40	62	8	19,840
	RT19	8T	5706.43	40	62	8	19,840

Figure 4.1.6: Block #4

Block No.	No.	No. Memory Type	Physical Size	Cell Size			
			X * Y (um2)	X(bit)	Y(bit)	Block (ea)	Total(bit)
Block #4	RT1	6T_A	16689.65	76	126	10	95,760
	RT2	6T_A	16689.65	76	126	10	95,760
	RT3	6T_A	13338.37	76	126	8	76,608
	RT4	6T_A	6649.16	76	126	4	38,304
	RT5	6T_A	3115.05	62	32	4	7,936
	RT6	6T_A	3115.05	62	32	4	7,936
	RT7	6T_A	1124.28	24	64	2	3,072
	RT8	6T_A	2001.54	32	126	2	8,064
	RT9	6T_A	2001.54	32	126	2	8,064
	RT10	6T_A	1954.21	48	64	2	6,144
	RT11	6T_A	2640	118	32	2	7,552
	RT12	6T_A	7183.83	90	126	4	45,360
	RT13	6T_A	7183.83	90	126	4	45,360
	RT14	6T_A	10748.74	82	126	6	61,992
	RT15	6T_A	10748.74	82	126	6	61,992
	RT16	6T_A	10748.74	82	126	6	61,992
	RT17	6T_A	10748.74	82	126	6	61,992
	RT18	6T_A	3895.97	118	80	2	18,880
	RT19	6T_A	3895.97	118	80	2	18,880
	RT20	6T_A	3895.97	118	80	2	18,880
	RT21	6T_A	3895.97	118	80	2	18,880

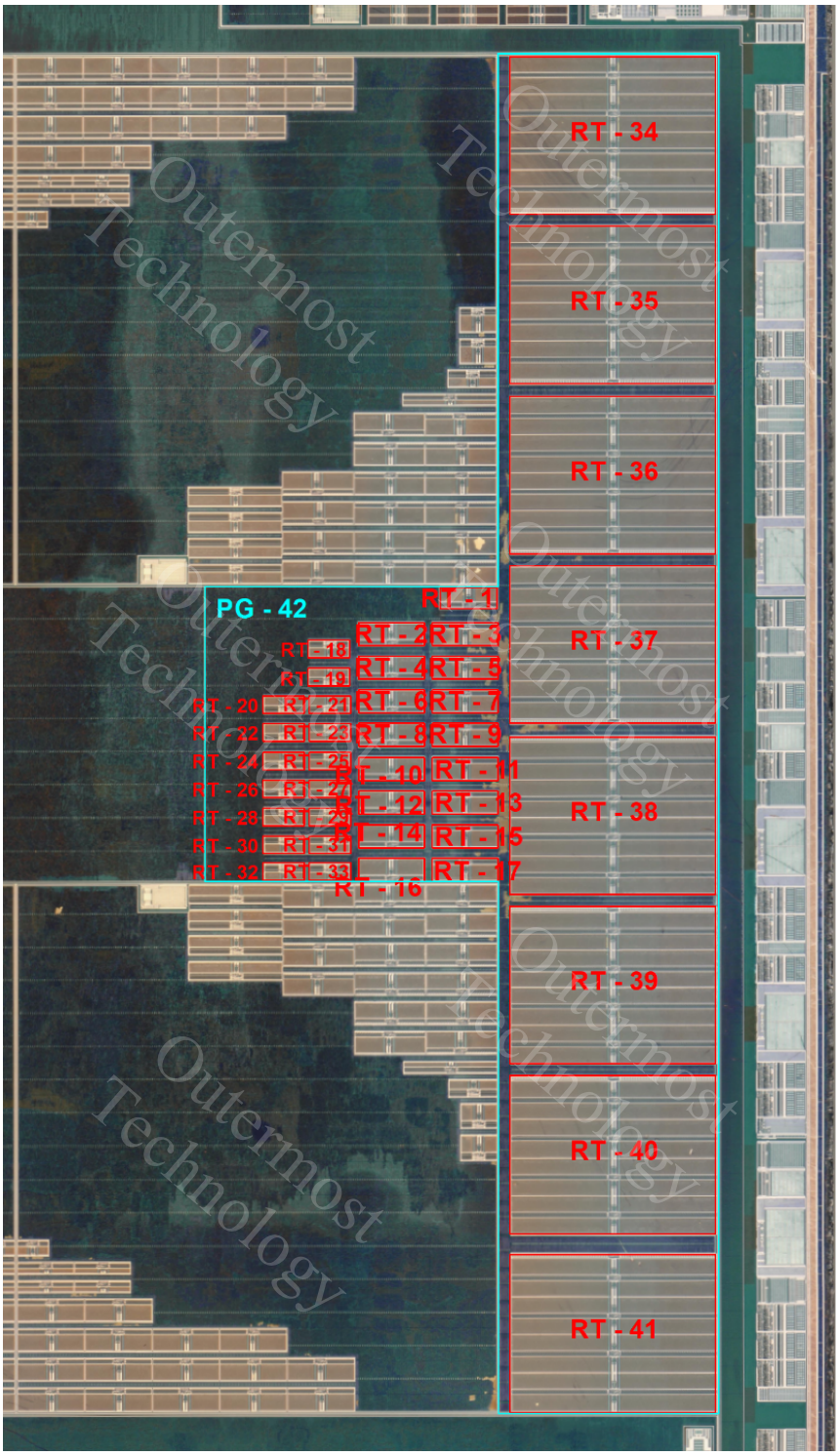

Figure 4.1.7: Block #5

Block No.	No.	No. Memory Type	Physical Size	Cell Size			
			X * Y (um2)	X(bit)	Y(bit)	Block (ea)	Total(bit)
Block #5	RT1	6T_A	2583.21	66	124	2	16,368
	RT2	6T_A	3159.09	78	126	2	19,656
	RT3	6T_A	3159.09	78	126	2	19,656
	RT4	6T_A	3159.09	78	126	2	19,656
	RT5	6T_A	3159.09	78	126	2	19,656
	RT6	6T_A	3159.09	78	126	2	19,656
	RT7	6T_A	3159.09	78	126	2	19,656
	RT8	6T_A	3159.09	78	126	2	19,656
	RT9	6T_A	3159.09	78	126	2	19,656
	RT10	6T_A	3159.09	78	126	2	19,656
	RT11	6T_A	3159.09	78	126	2	19,656
	RT12	6T_A	3159.09	78	126	2	19,656
	RT13	6T_A	3159.09	78	126	2	19,656
	RT14	6T_A	3159.09	78	126	2	19,656
	RT15	6T_A	3159.09	78	126	2	19,656
	RT17	6T_A	3159.09	78	126	2	19,656
	RT18	6T_A	3159.09	78	126	2	19,656
	RT20	6T_A	1519.94	38	64	2	4,864
	RT21	6T_A	1519.95	38	64	2	4,864
	RT22	6T_A	1519.94	38	64	2	4,864
	RT23	6T_A	1519.93	38	64	2	4,864
	RT24	6T_A	1519.94	38	64	2	4,864
	RT25	6T_A	1519.93	38	64	2	4,864
	RT26	6T_A	1519.94	38	64	2	4,864
	RT27	6T_A	1519.93	38	64	2	4,864
	RT28	6T_A	1519.94	38	64	2	4,864
	RT29	6T_A	1519.93	38	64	2	4,864
	RT30	6T_A	1519.94	38	64	2	4,864
	RT31	6T_A	1519.93	38	64	2	4,864
	RT32	6T_A	1519.94	38	64	2	4,864
	RT33	6T_A	1519.93	38	64	2	4,864
	RT34	6T_A	1519.94	38	64	2	4,864
	RT35	6T_A	1519.93	38	64	2	4,864
	RT36	6T_A	67731.82	284	126	16	572,544
	RT37	6T_A	67731.82	284	126	16	572,544
	RT38	6T_A	67731.82	284	126	16	572,544
	RT39	6T_A	67731.82	284	126	16	572,544
	RT40	6T_A	67731.82	284	126	16	572,544
	RT41	6T_A	67731.82	284	126	16	572,544
	RT42	6T_A	67731.82	284	126	16	572,544
	RT43	6T_A	67731.99	284	126	16	572,544

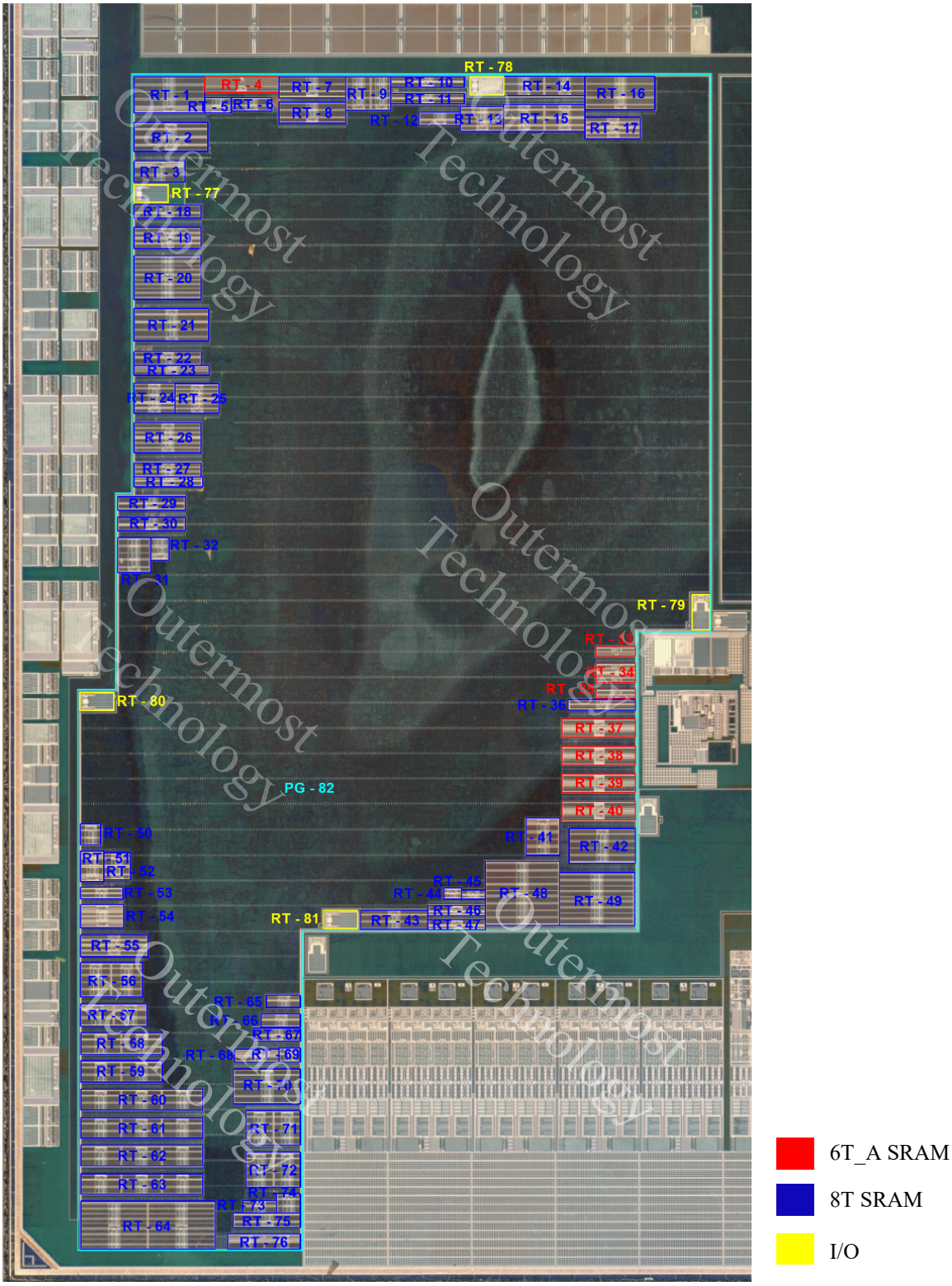

Figure 4.1.8: Block #6

Block No.	No.	No. Memory Type	Physical Size	Cell Size			
			X * Y (um2)	X(bit)	Y(bit)	Block (ea)	Total(bit)
Block #6	RT1	8T	9856.75	70	62	8	34,720
	RT2	8T	8240.44	74	62	4	18,352
	RT3	8T	4062.41	46	62	4	11,408
	RT4	6T_A	4426.09	130	94	2	24,440
	RT5	8T	1545.16	16	62	2	1,984
	RT6	8T	2021.72	32	62	4	7,936
	RT7	8T	5419.89	66	62	4	16,368
	RT8	8T	5419.89	66	62	4	16,368
	RT9	8T	5811.64	14	62	4	3,472
				12	62	4	2,976
				8	62	4	1,984
				6	62	4	1,488
	RT10	8T	2975.31	74	32	2	4,736
	RT11	8T	2975.31	74	62	2	9,176
	RT12	8T	2072.85	32	62	2	3,968
	RT13	8T	4101.4	36	36	8	10,368
	RT14	8T	6019.35	32	62	8	15,872
	RT15	8T	8480.77	32	62	8	15,872
	RT16	8T	8972.35	70	62	8	34,720
	RT17	8T	4538.98	50	32	4	6,400
	RT18	8T	3374.65	64	62	2	7,936
	RT19	8T	5522.15	66	32	4	8,448
	RT20	8T	11248.82	66	34	16	35,904
	RT21	8T	9355.91	72	62	6	26,784
	RT22	8T	3548.98	64	64	2	8,192
	RT23	8T	2867.58	72	10	4	2,880
	RT24	8T	4782.04	0	0	1	0
	RT25	8T	5029.65	36	34	8	9,792
	RT26	8T	7692.41	66	34	8	17,952
	RT27	8T	3641.07	66	34	4	8,976
	RT28	8T	2564.9	66	16	2	2,112
	RT29	8T	3548.98	66	62	2	8,184
	RT30	8T	3548.98	66	62	2	8,184
	RT31	8T	4406.07	22	62	8	10,912
	RT32	8T	1573.99	6	60	1	360
				4	60	1	240
	RT33	6T_A	1388.88	58	34	2	3,944
	RT34	6T_A	2898.54	58	34	4	7,888
	RT35	6T_A	1388.88	58	34	2	3,944
	RT36	8T	2837.24	66	32	2	4,224
	RT37	6T_A	5234.94	128	10	4	5,120
	RT38	6T_A	5234.94	128	10	4	5,120
	RT39	6T_A	5234.94	128	10	4	5,120
	RT40	6T_A	5234.94	128	10	4	5,120
	RT41	8T	4769.29	22	62	8	10,912
	RT42	8T	8766.92	66	62	8	32,736
	RT43	8T	4923.14	68	62	4	16,864
	RT44	8T	778.34	4	32	2	256
	RT45	8T	862.85	12	16	2	384

Block No.	No.	No. Memory Type	Physical Size	Cell Size			
			X * Y (um2)	X(bit)	Y(bit)	Block (ea)	Total(bit)
Block #6	RT46	8T	2244	54	16	2	1,728
	RT47	8T	2244	54	16	2	1,728
	RT48	8T	18279.56	74	62	16	73,408
	RT49	8T	15312.9	76	46	16	55,936
	RT50	8T	1640.44	8	62	4	1,984
	RT51	8T	2733.76	10	62	4	2,480
	RT52	8T	2785.65	14	62	4	3,472
	RT53	8T	1842.08	34	32	2	2,176
	RT54	8T	3819.2	34	16	4	2,176
	RT55	8T	5674.48	66	32	4	8,448
	RT56	8T	8142.12	20	62	16	19,840
	RT57	8T	5709.68	24	62	8	11,904
	RT58	8T	6734.73	32	62	8	15,872
	RT59	8T	6734.73	32	62	8	15,872
	RT60	8T	9595.33	32	62	12	23,808
	RT61	8T	9595.33	32	62	12	23,808
	RT62	8T	9595.33	32	62	12	23,808
	RT63	8T	9595.33	32	62	12	23,808
	RT64	8T	24754.84	66	40	32	84,480
	RT65	8T	1617.99	24	62	2	2,976
	RT66	8T	1982.73	30	62	2	3,720
	RT67	8T	2383.28	40	62	1	2,480
	RT68	8T	2175.12	36	32	2	2,304
	RT69	8T	1136.41	10	62	1	620
				8	62	1	496
	RT70	8T	8999.06	64	62	8	31,744
	RT71	8T	7192.02	16	62	16	15,872
	RT72	8T	7399.89	16	62	16	15,872
	RT73	8T	1624.96	24	62	2	2,976
	RT74	8T	1769.41	12	62	4	2,976
	RT75	8T	3681.43	66	62	2	8,184
	RT76	8T	4153.45	26	62	4	6,448

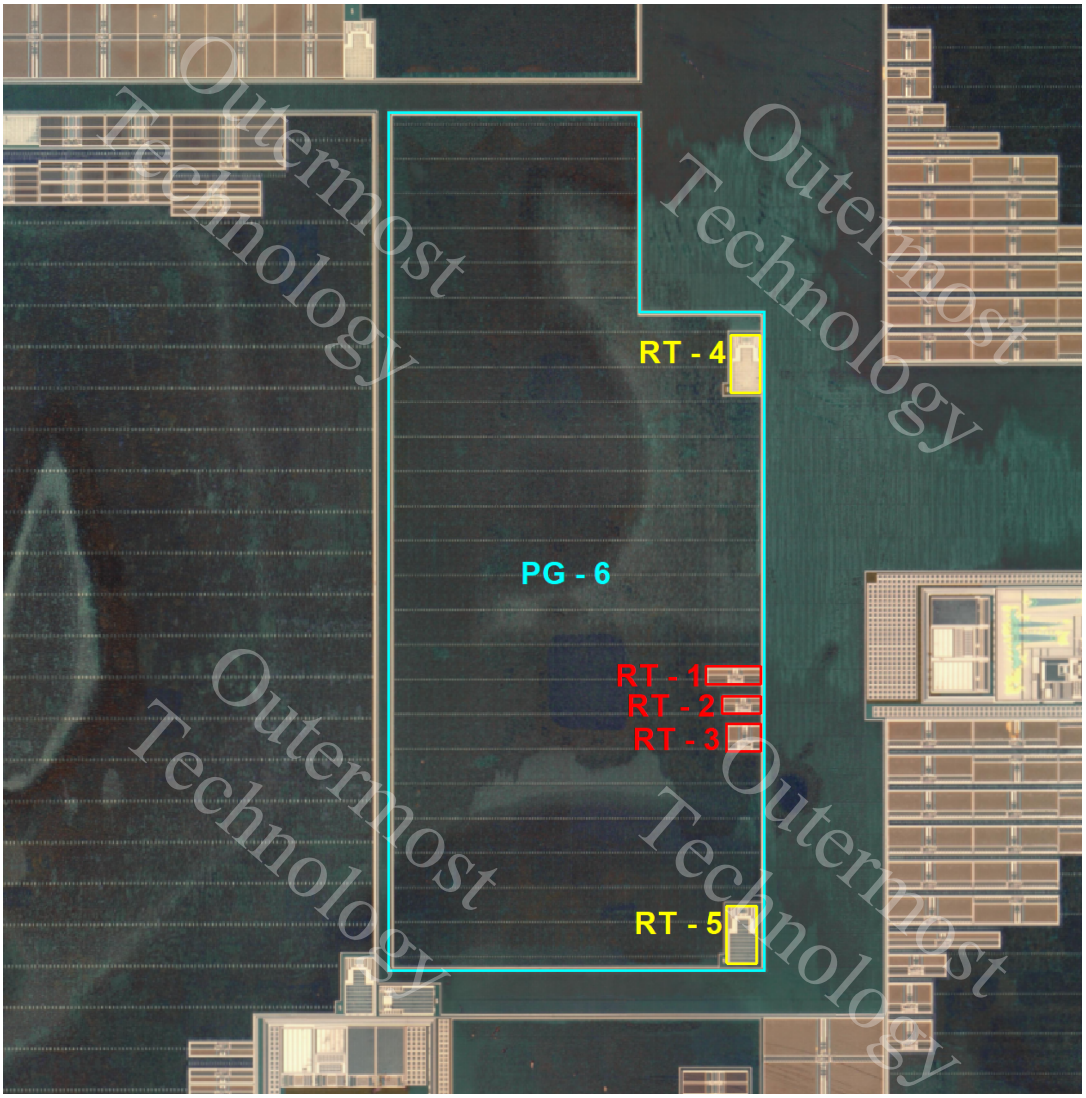

Figure 4.1.9: Block #7

Block No.	No.	No. Memory Type	Physical Size	Cell Size			
			X * Y (um2)	X(bit)	Y(bit)	Block (ea)	Total(bit)
Block #7	RT1	6T_A	1444.41	44	32	2	2,816
	RT2	6T_A	964.97	24	32	2	1,536
	RT3	6T_A	1412.4	20	94	2	3,760

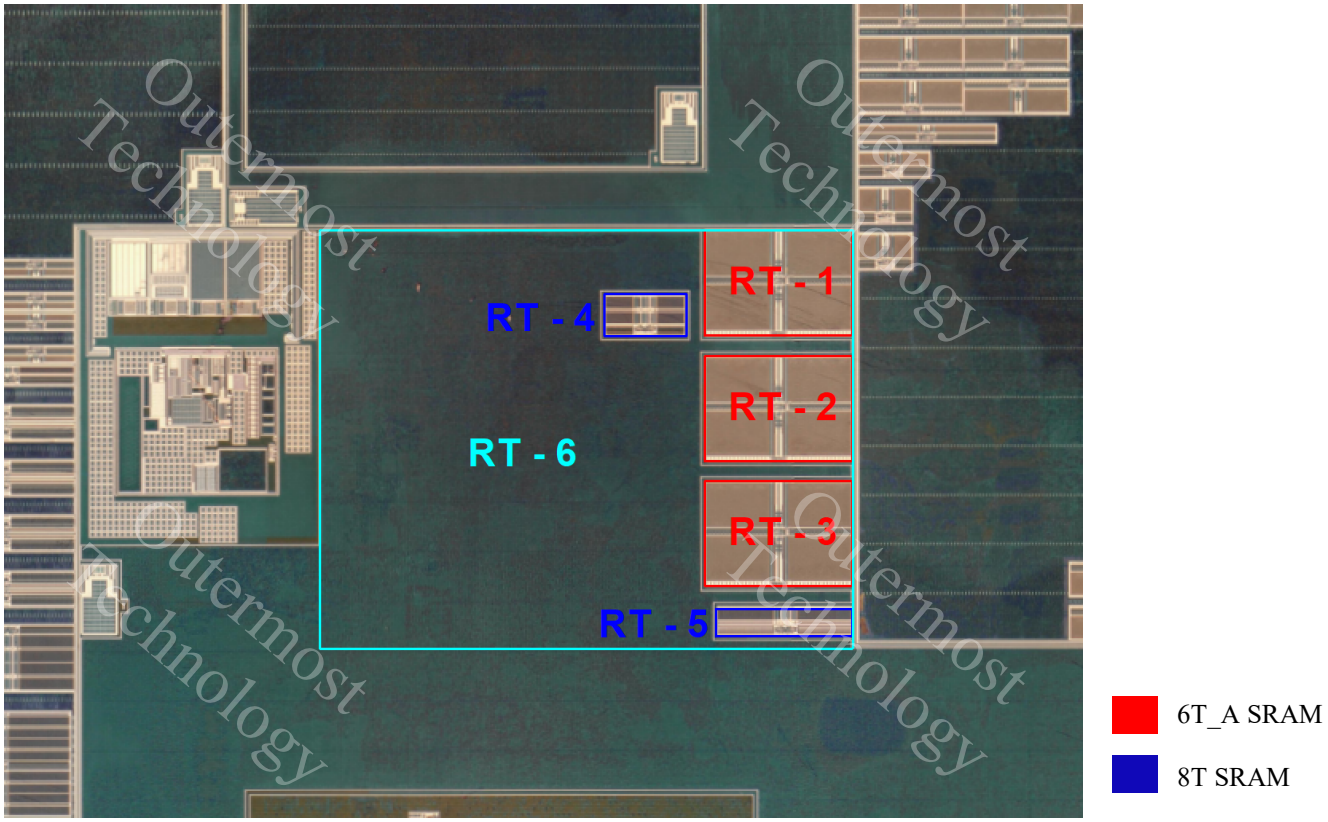

Figure 4.1.10: Block #8

Block No.	No.	No. Memory Type	Physical Size	Cell Size			
			X * Y (um2)	X(bit)	Y(bit)	Block (ea)	Total(bit)
Block #8	RT1	6T_A	14847.12	130	252	4	131,040
	RT2	6T_A	14847.12	130	252	4	131,040
	RT3	6T_A	14847.12	130	252	4	131,040
	RT4	8T	3302.86	34	62	4	8,432
	RT5	8T	3604.73	68	62	2	8,432

4.2 Cell Size

- 6T_A SRAM : 0.480um x 0.166um (0.0797um^2)

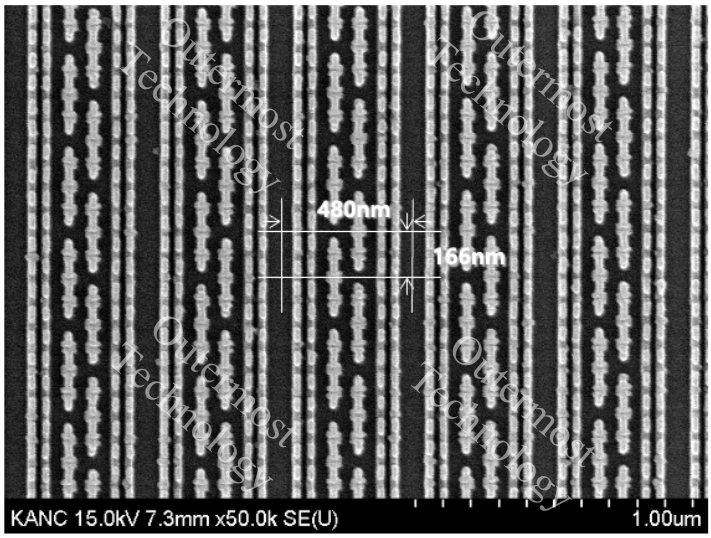

Figure 4.2.1: 6T_A SRAM cell

- 6T_B SRAM : 0.384um x 0.168um (0.0645um^2)

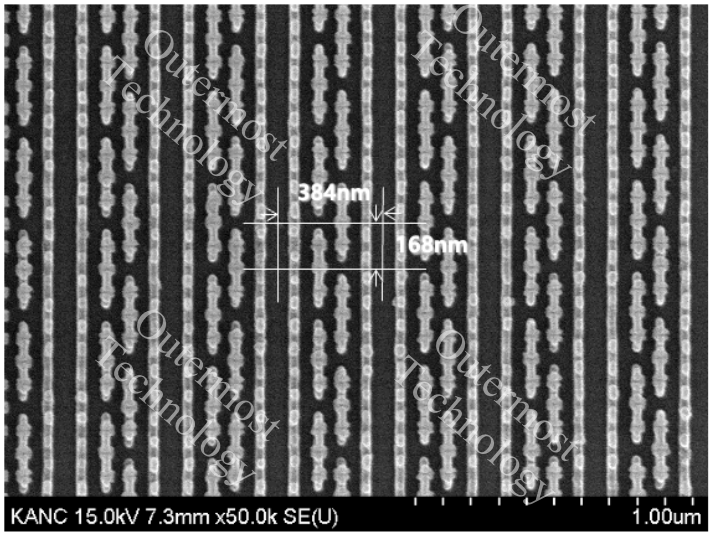

Figure 4.2.2: 6T_B SRAM cell

- 8T SRAM : 0.815um x 0.167um (0.136um^2)

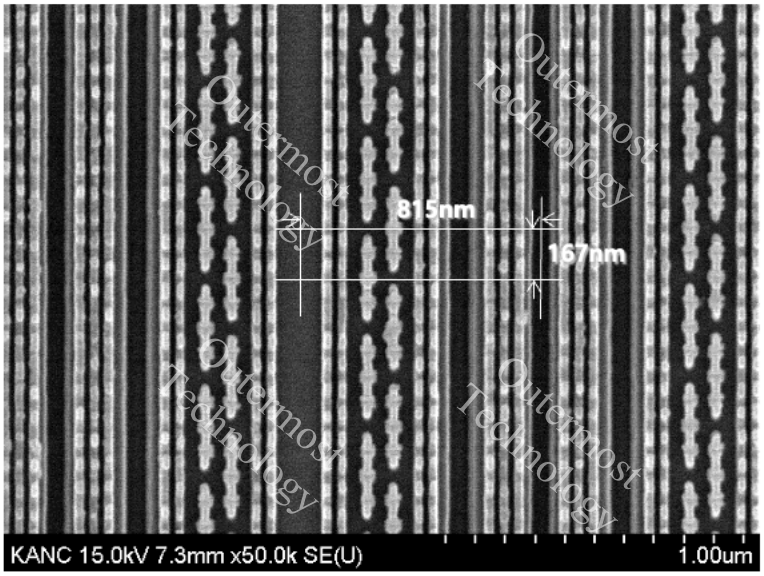

Figure 4.2.3: 8T SRAM cell

- ROM : 0.383um x 0.250um (0.0958um^2)

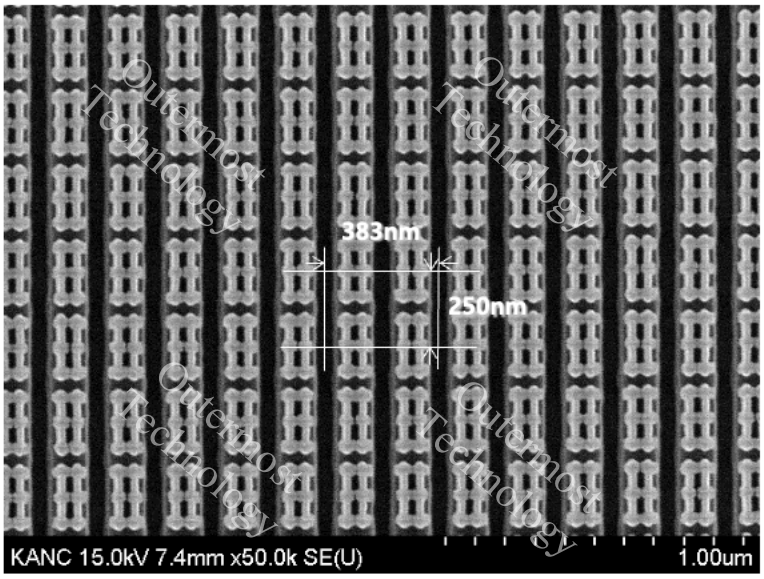

Figure 4.2.4: ROM

4.3 SRAM Cell Layout

- 6T_A SRAM

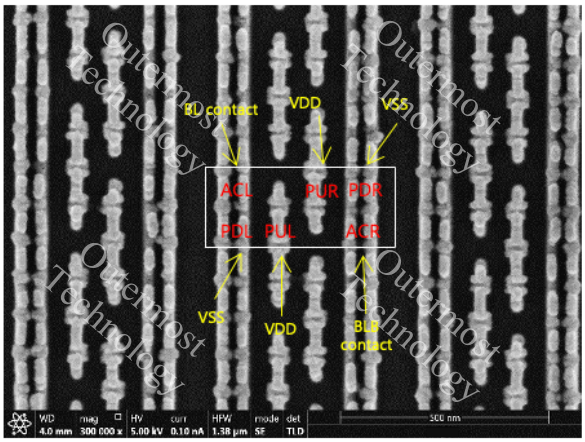

Figure 4.3.1: Active Level

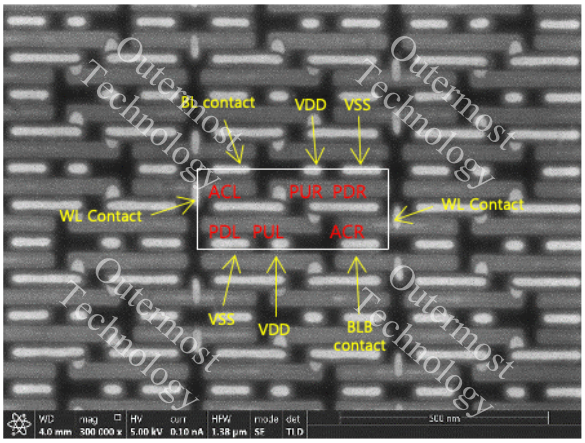

Figure 4.3.2: poly & contact Level

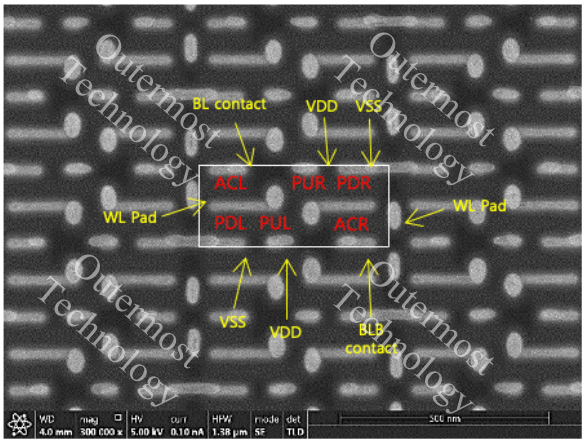

Figure 4.3.3: Metal-1 & Via-1 level

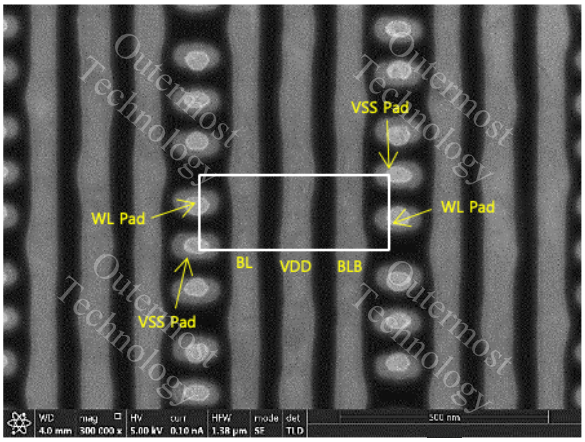

Figure 4.3.4: Metal-2 & Via-2 Level

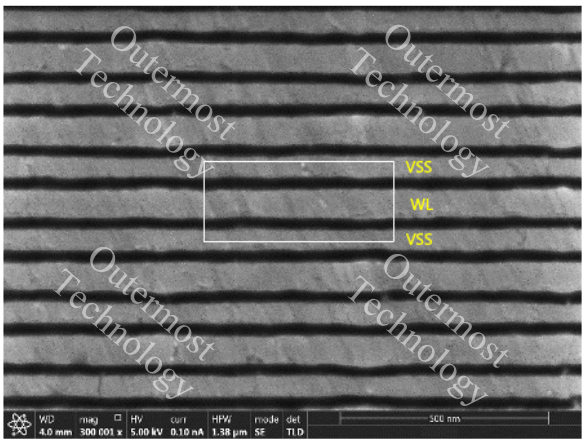

Figure 4.3.5: Metal-3 Level

- 6T_B SRAM

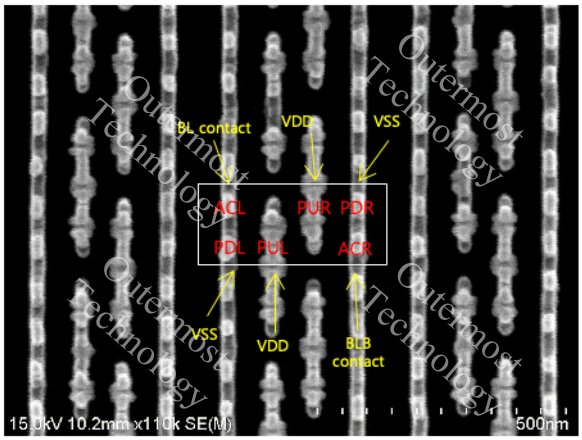

Figure 4.3.6: Active Level

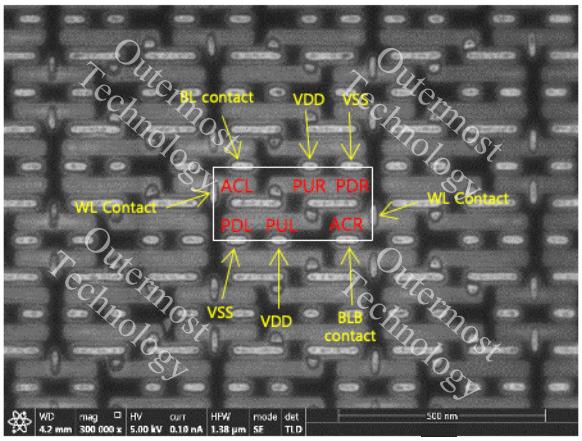

Figure 4.3.7: poly & contact Level

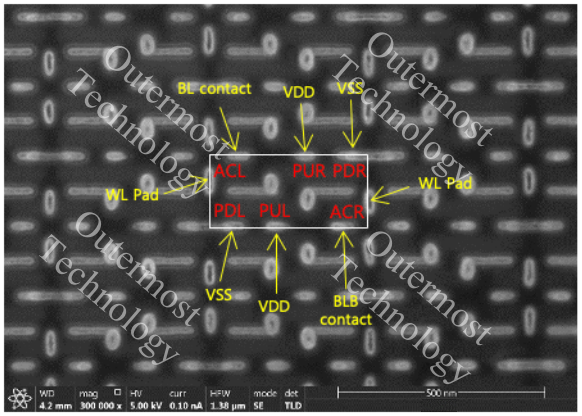

Figure 4.3.8: Metal-1 & Via-1 level

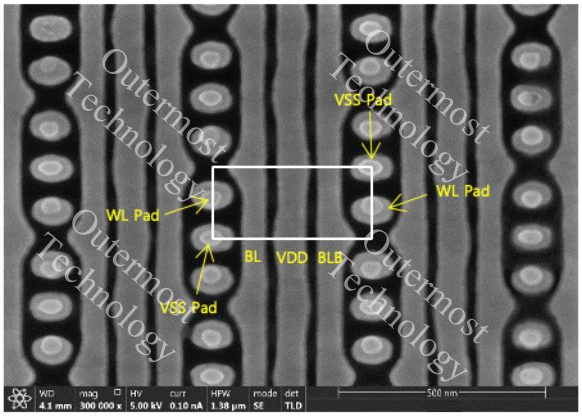

Figure 4.3.9: Metal-2 & Via-2 Level

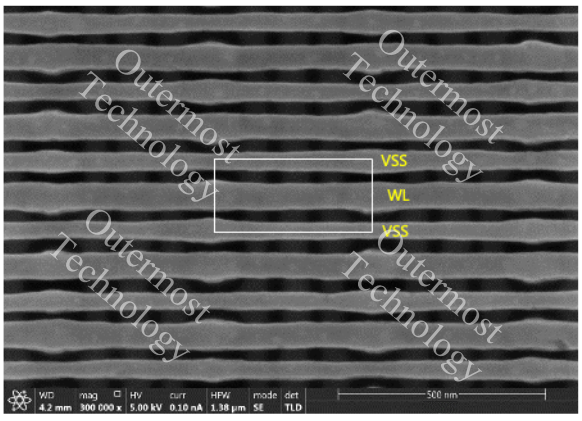

Figure 4.3.10: Metal-3 Level

- 8T_SRAM

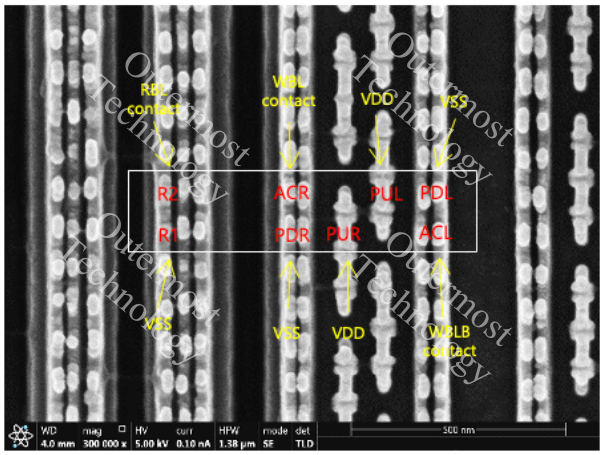

Figure 4.3.11: Active Level

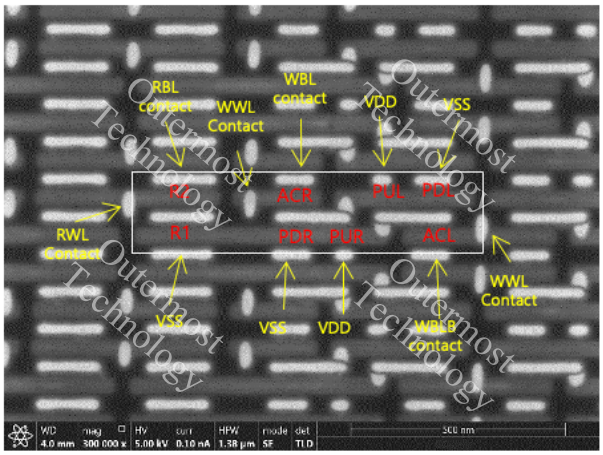

Figure 4.3.12: poly & contact level

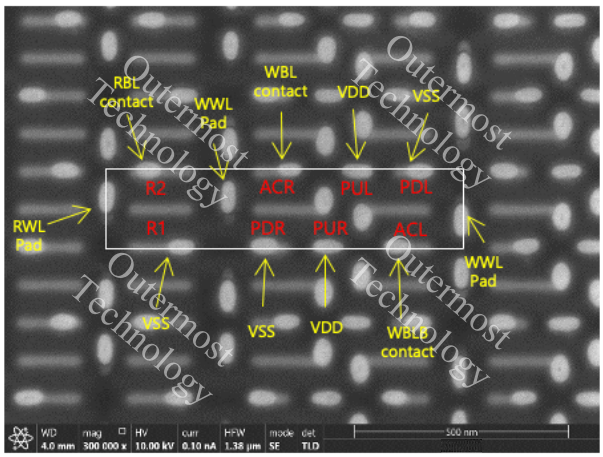

Figure 4.3.13: Metal-1 & Via-1 level

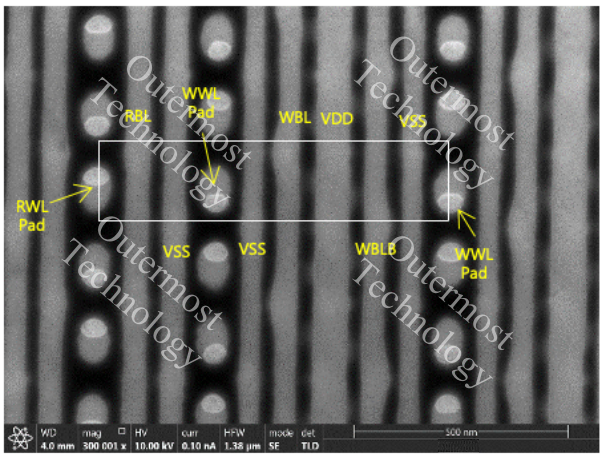

Figure 4.3.14: Metal-2 & Via-2 Level

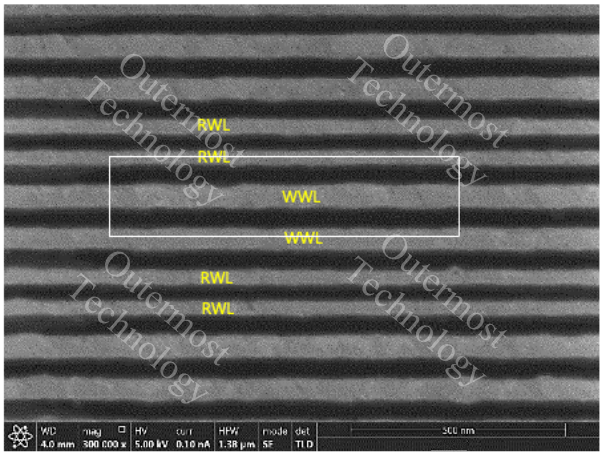

Figure 4.3.15: Metal-3 Level